

# Round Rock 13.3" Schematics Document

## Haswell ULT

**2013-06-28**

**REV : SSI**

[www.aitech1.ru](http://www.aitech1.ru)

*DY : None Installed*

*XDP: For CPU XDP Debug Port installed*

*PCH\_XDP: For PCH XDP Debug Port installed*

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size  
A3

Document Number

**Round Rock 13.3" UMA**

Rev  
**X00**

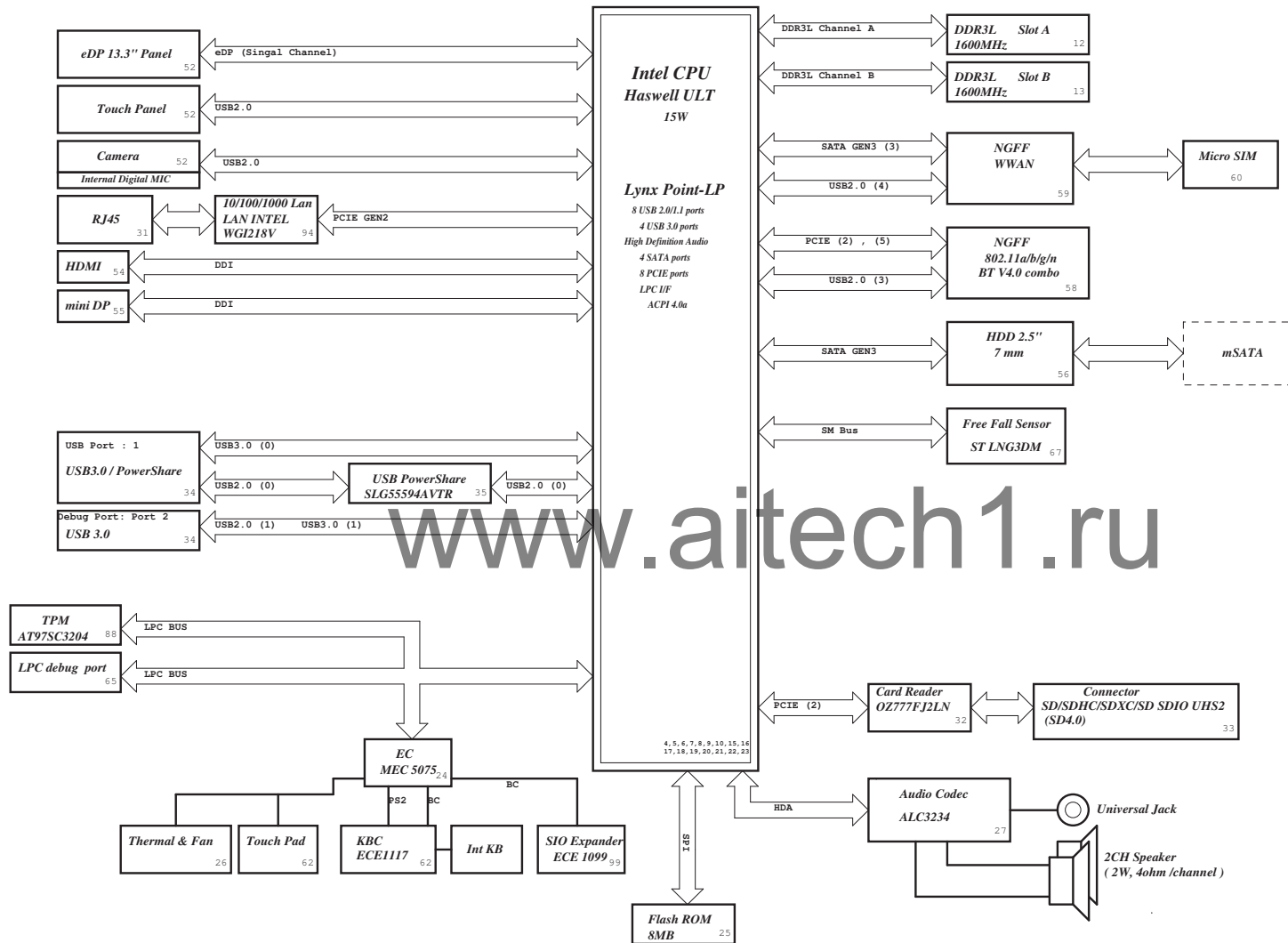
Date: Friday, June 28, 2013

Sheet 1 of 107

# Round Rock 13.3" Block Diagram

Project code : 91.40A01.001  
PCB P/N : 13229  
Revision : X00

CHARGER BQ24715 44	
INPUTS	OUTPUTS
AD+ BT+	DCRATOUT
SYSTEM DC/DC TPS51275 45	
INPUTS	OUTPUTS
DCRATOUT	3.3V_AUX_S5 3.3V_V5 5V_V5
CPU DC/DC TPS51622 46-47	
INPUTS	OUTPUTS
DCRATOUT	VCC_CORE
SYSTEM DC/DC TPS51363 48	
INPUTS	OUTPUTS
DCRATOUT	ID05V_M
SYSTEM DC/DC TPS51363 & APL5338 49	
INPUTS	OUTPUTS
DCRATOUT	ID05V_S3 ID0675V_S0 DDR_VREF_S3
Load Switches 36	
INPUTS	OUTPUTS
5V_S3 3.3V_S5	5V_S0 3.3V_S0 3.3V_SS_PCH 3.3V_M 3.3V_LAN ID05V_MODPHY ID05V_S0
PCB LAYER(FR4-6 Layer)	
L1:Top L2:Power/GND L3:Signal L4:Signal L5:Power/GND	L6:Bottom



5

4

3

2

1

D

C

B

A

(Blanking)  
www.aitech1.ru

&lt;Core Design&gt;

**Wistron Corporation**21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**CPU (PCIE/DMI/FDI)**Size  
A4

Document Number

**Round Rock 13.3" UMA**

Rev

**X00**

Date: Friday, June 28, 2013

Sheet 3 of 107



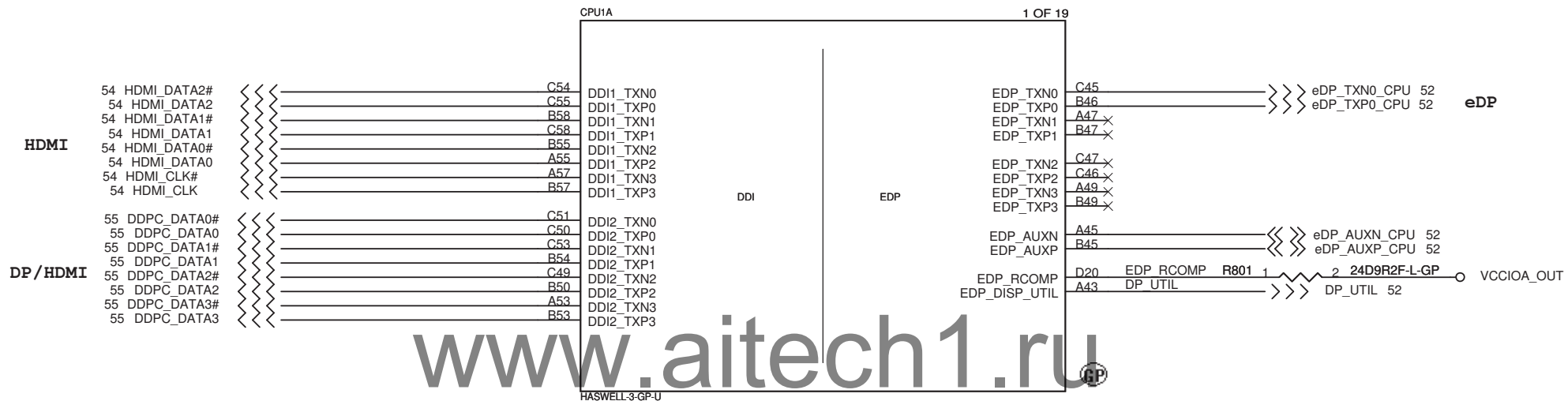








SSID = CPU



DDI	HDMI	Display Port
DDI_TXN0	HDMI_DATA2_N	DP_LANE0_N
DDI_TXP0	HDMI_DATA2_P	DP_LANE0_P
DDI_TXN1	HDMI_DATA1_N	DP_LANE1_N
DDI_TXP1	HDMI_DATA1_P	DP_LANE1_P
DDI_TXN2	HDMI_DATA0_N	DP_LANE2_N
DDI_TXP2	HDMI_DATA0_P	DP_LANE2_P
DDI_TXN3	HDMI_CLK_N	DP_LANE3_N
DDI_TXP3	HDMI_CLK_P	DP_LANE3_P

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**CPU (DDI/EDP)**

Size  
A4

Document Number

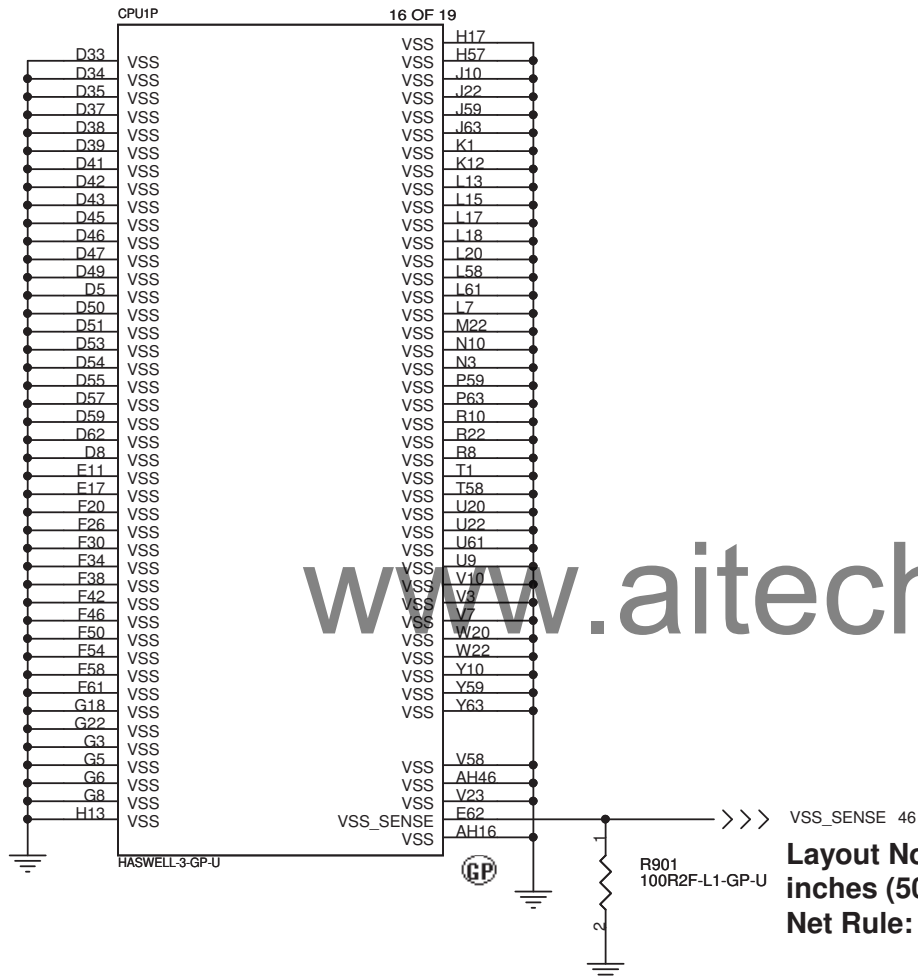
**Round Rock 13.3" UMA**

Rev  
X00

Date: Friday, June 28, 2013

Sheet 8 of 107

SSID = CPU



**Layout Note: R901 should be placed within 2 inches (50.8 mm) of the processor.**  
**Net Rule: VCC\_SENSE and VSS\_SENSE differential signals**

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**CPU (VSS)**

Size  
A4

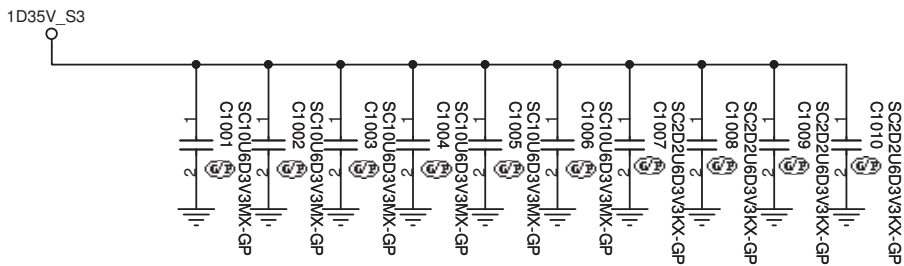
Document Number

**Round Rock 13.3" UMA**

Rev  
**X00**

Date: Friday, June 28, 2013

Sheet 9 of 107



www.aitech1.ru

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**CPU (Power CAP1)**

Size  
A4

Document Number

**Round Rock 13.3" UMA**

Rev  
X00

Date: Friday, June 28, 2013

Sheet 10 of 107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***CPU (Power CAP2)***

Size  
A

Document Number

***Round Rock 13.3" UMA***

Rev

***X00***

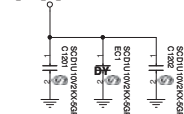
Date: Friday, June 28, 2013

Sheet 11 of 107

**Layout Note:**

Place these caps close to VREF\_CA

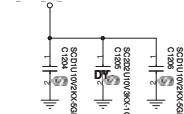
M\_VREF\_CA\_DIMMA



**Layout Note:**

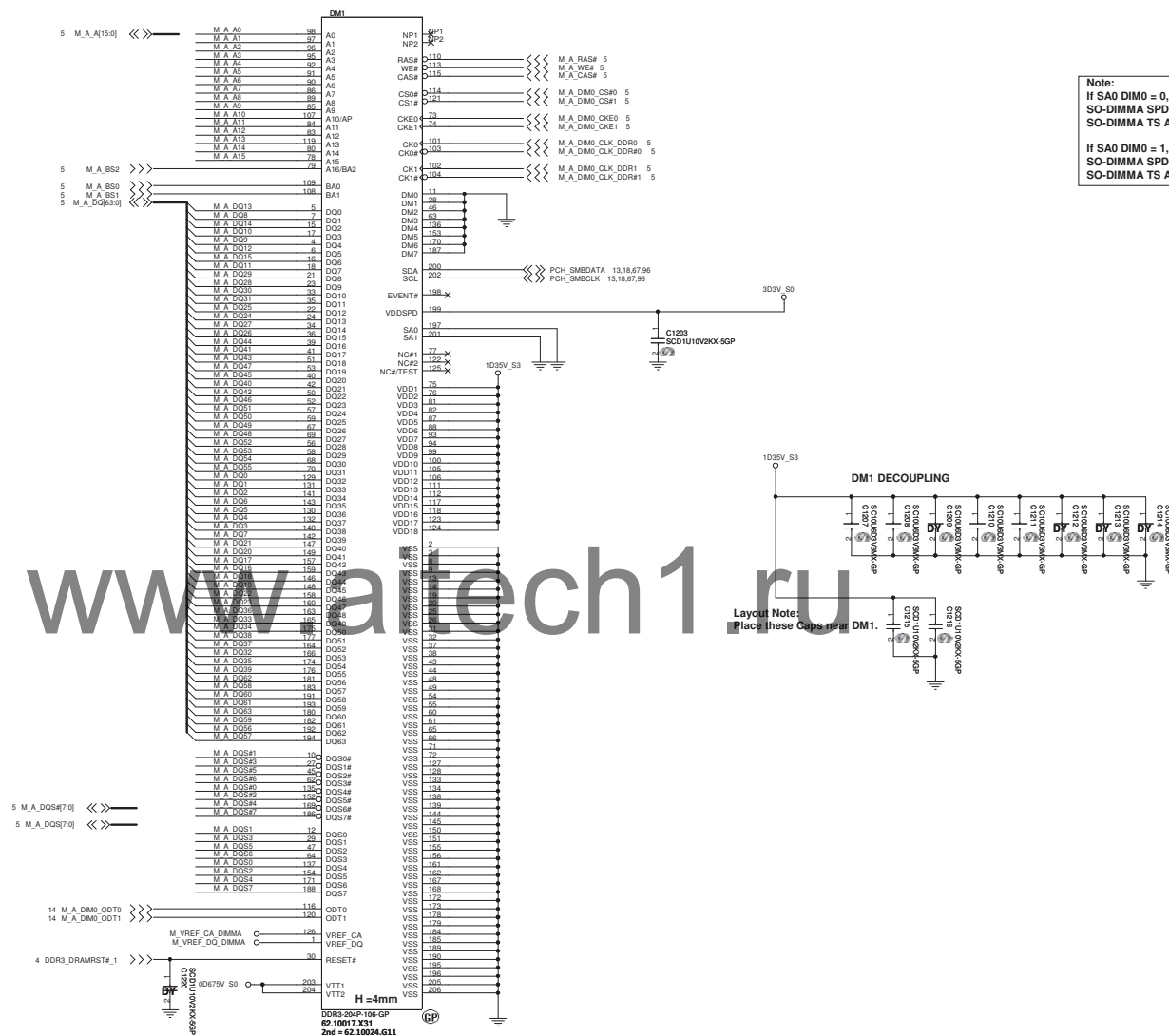
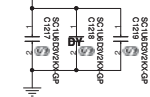
Place these caps close to VREF\_DQ

M VREF DQ DIMMA



0D675V\_S0

Place these caps  
close to VTT1 and VTT2



**Note:**  
If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30  
  
If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32

Layout Note:  
Place these Caps near DM1.

&lt;Core Design&gt;

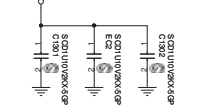


Title			
<b>DDR3L-SODIMM1</b>			
Size A2	Document Number	<b>Round Rock 13.3" UMA</b>	Rev X0
Date: Friday, June 28, 2013	Sheet	12	of 107

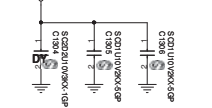


SSID = MEMORY

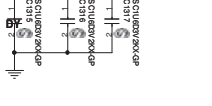
Layout Note:  
Place these caps close to VREF\_CA  
M\_VREF\_CA\_DIMMB



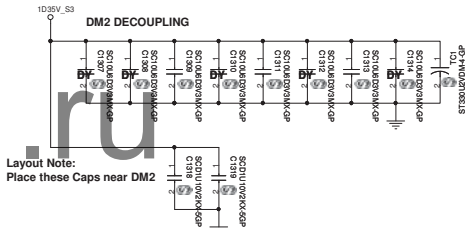
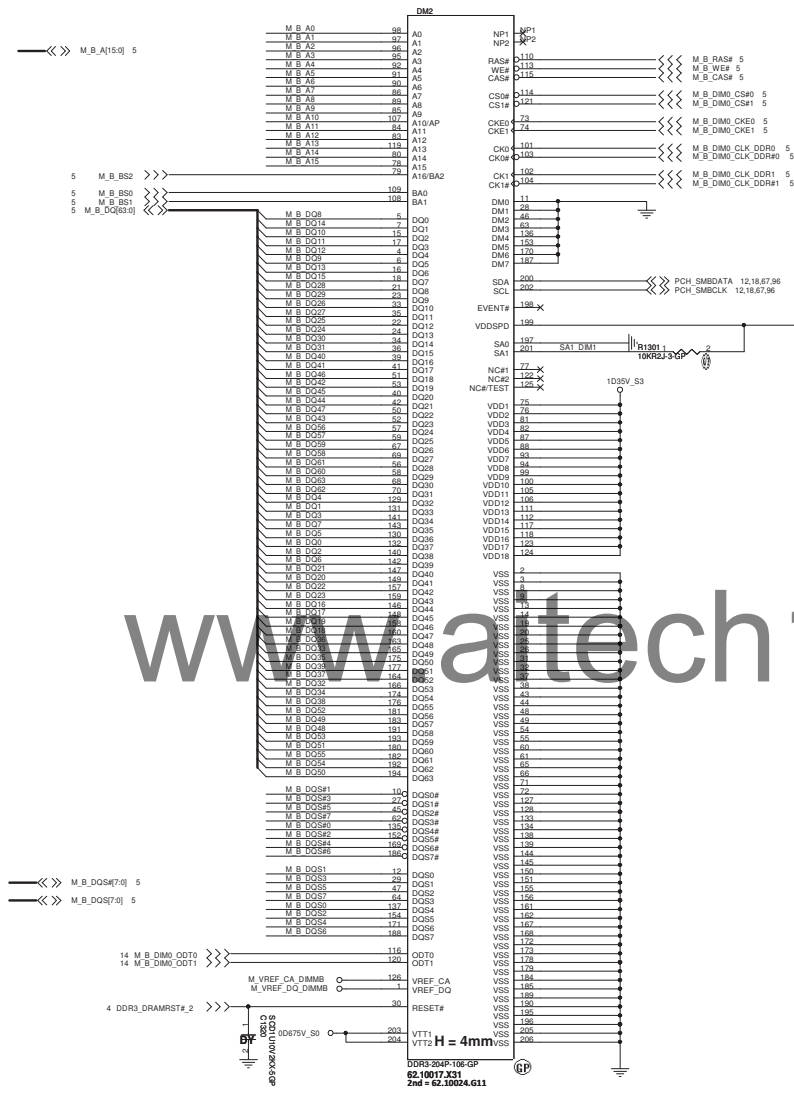
Layout Note:  
Place these caps close to VREF\_DQ  
M\_VREF\_DQ\_DIMMB



Place these caps  
close to VTT1 and VTT2.



DQS1	DQ0	M_B_DQ8
	DQ1	M_B_DQ14
	DQ2	M_B_DQ10
	DQ3	M_B_DQ11
	DQ4	M_B_DQ12
	DQ5	M_B_DQ9
	DQ6	M_B_DQ13
	DQ7	M_B_DQ15
DQS3	DQ8	M_B_DQ28
	DQ9	M_B_DQ29
	DQ10	M_B_DQ26
	DQ11	M_B_DQ27
	DQ12	M_B_DQ25
	DQ13	M_B_DQ24
	DQ14	M_B_DQ30
	DQ15	M_B_DQ31
DQS5	DQ16	M_A_DQ40
	DQ17	M_A_DQ41
	DQ18	M_A_DQ46
	DQ19	M_A_DQ42
	DQ20	M_A_DQ45
	DQ21	M_A_DQ44
	DQ22	M_A_DQ47
	DQ23	M_A_DQ43
DQS7	DQ24	M_A_DQ56
	DQ25	M_A_DQ57
	DQ26	M_A_DQ59
	DQ27	M_A_DQ58
	DQ28	M_A_DQ61
	DQ29	M_A_DQ60
	DQ30	M_A_DQ63
	DQ31	M_A_DQ62
DQS0	DQ32	M_A_DQ4
	DQ33	M_A_DQ1
	DQ34	M_A_DQ3
	DQ35	M_A_DQ7
	DQ36	M_A_DQ5
	DQ37	M_A_DQ0
	DQ38	M_A_DQ2
	DQ39	M_A_DQ6
DQS2	DQ40	M_A_DQ21
	DQ41	M_A_DQ20
	DQ42	M_A_DQ22
	DQ43	M_A_DQ23
	DQ44	M_A_DQ16
	DQ45	M_A_DQ17
	DQ46	M_A_DQ19
	DQ47	M_A_DQ18
DQS4	DQ48	M_A_DQ36
	DQ49	M_A_DQ33
	DQ50	M_A_DQ35
	DQ51	M_A_DQ37
	DQ52	M_A_DQ39
	DQ53	M_A_DQ32
	DQ54	M_A_DQ34
	DQ55	M_A_DQ38
DQS6	DQ56	M_A_DQ52
	DQ57	M_A_DQ49
	DQ58	M_A_DQ48
	DQ59	M_A_DQ51
	DQ60	M_A_DQ53
	DQ61	M_A_DQ55
	DQ62	M_A_DQ54
	DQ63	M_A_DQ50

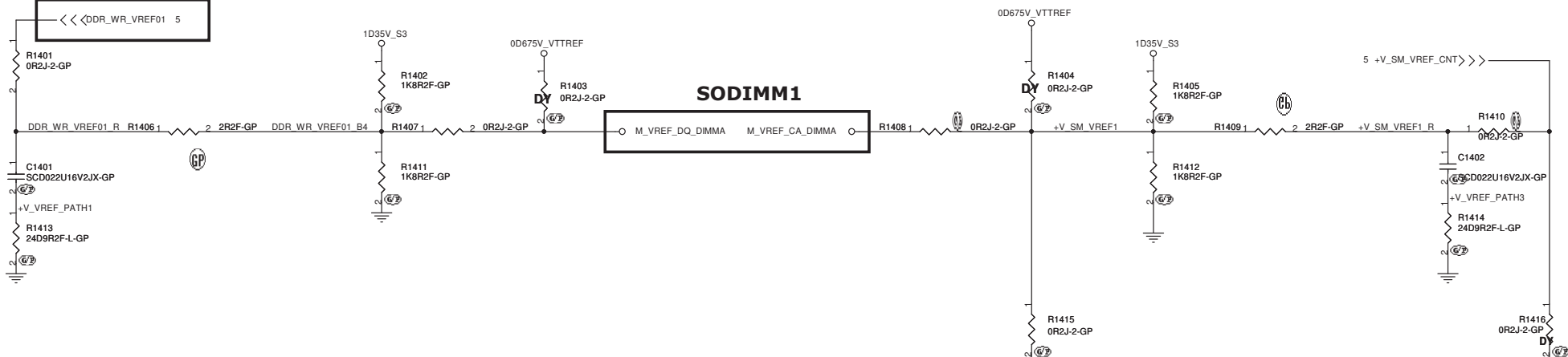


Layout Note:  
Place these Caps near DM2

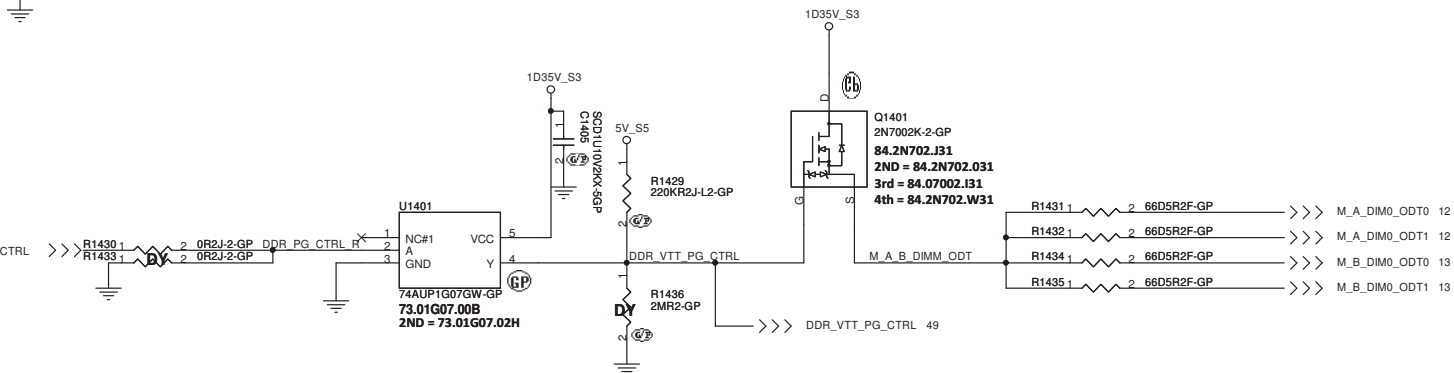
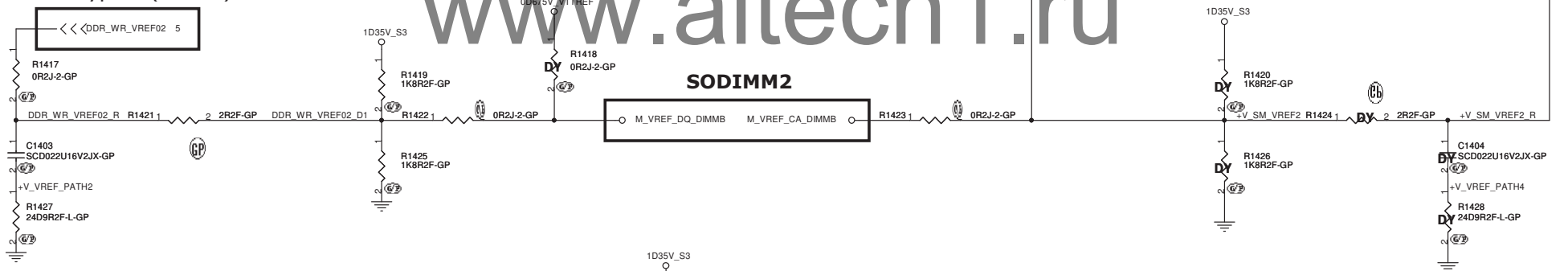
Note:  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34  
SO-DIMMB is placed farther from  
the Processor than SO-DIMMA

# SSID = MEMORY VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

## SA\_DIMM\_VREFDQ Driven by process (PIN#AR51)

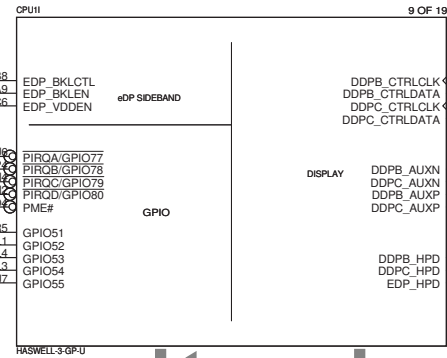
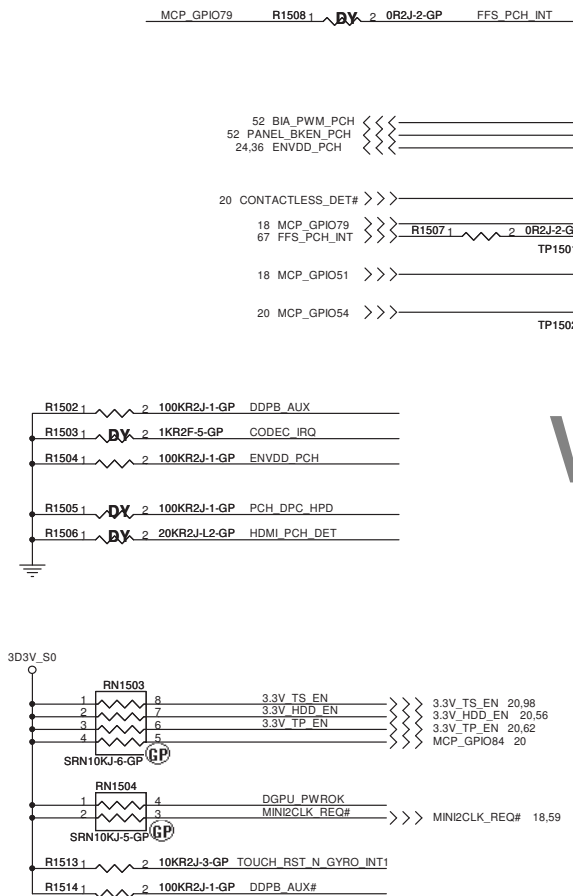


## SB\_DIMM\_VREFDQ Driven by process (PIN#AP51)

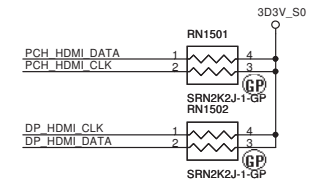


<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		<b>M1 &amp; M3 Implementation</b>	
Size	Document Number	Rev	
A3			X00
Date: Friday, June 28, 2013		Sheet	14 of 107



www.aitech1.ru

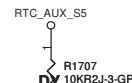
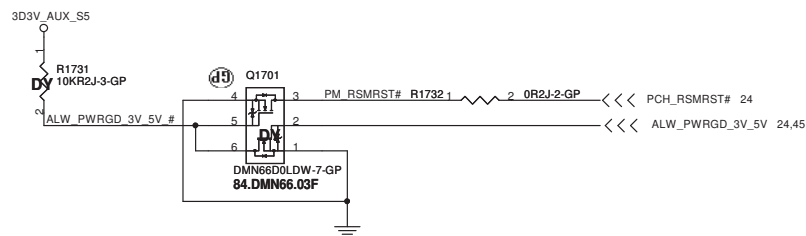
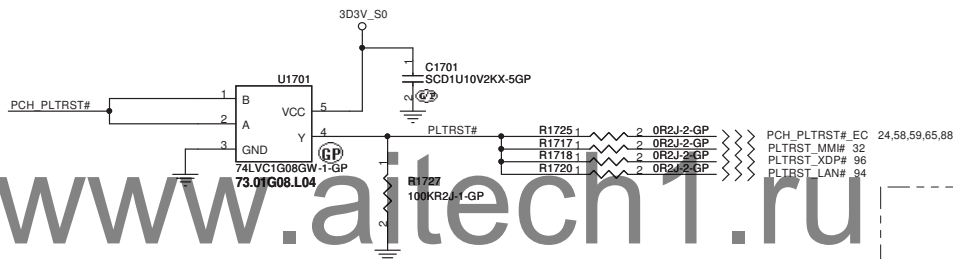
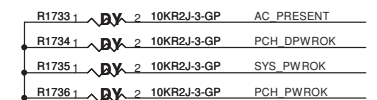
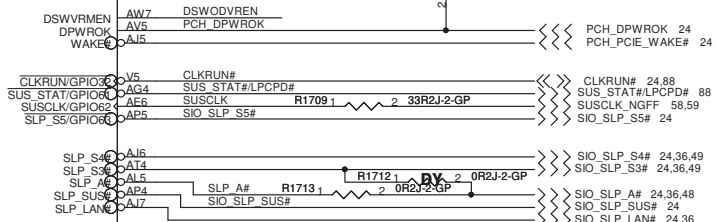
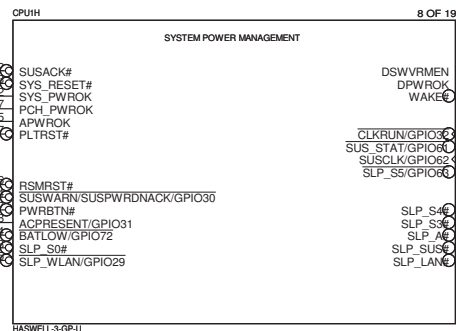


<Core Design>

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>CPU (DDI/PCI)</b>		
Size A3	Document Number <b>Round Rock 13.3" UMA</b>	Rev <b>X00</b>
Date: Friday, June 28, 2013	Sheet 15 of 107	



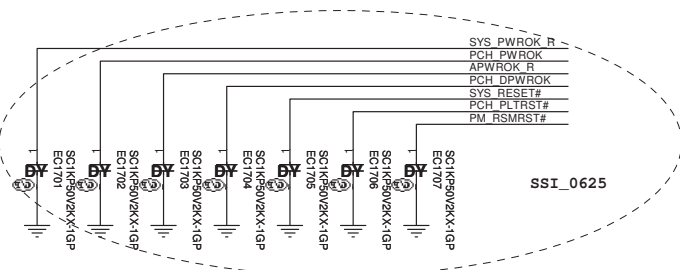
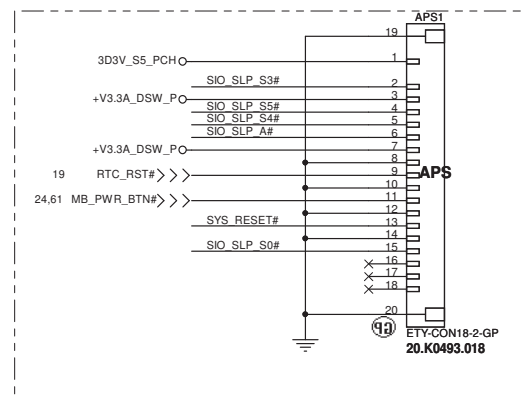
**NOTE:**  
PWRBTN# Integrated Pull-Up.



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

The diagram illustrates the electrical connection between the DSWODVREN signal and the RTC\_AUX\_S signal. The DSWODVREN line is shown with a pull-up resistor R1723 (330KR2J-1-L1-GP) connected to ground. The RTC\_AUX\_S line is shown with a pull-down resistor R1721 (330KR2J-1-L1-GP) connected to the DSWODVREN line. A 'Dx' symbol is present on the DSWODVREN line.



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**CPU (PM)**

Size

Document Number	
-----------------	--

Rev

### Round Rock 13.3" UMA

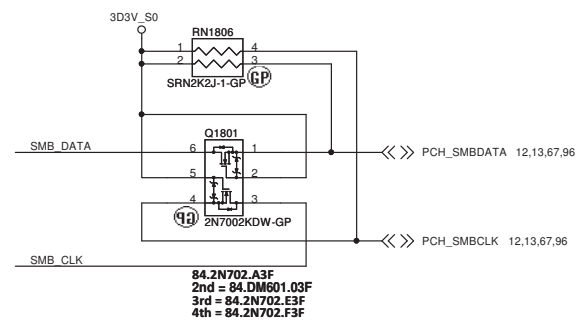
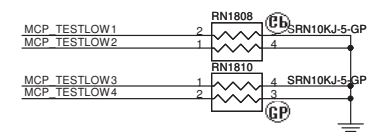
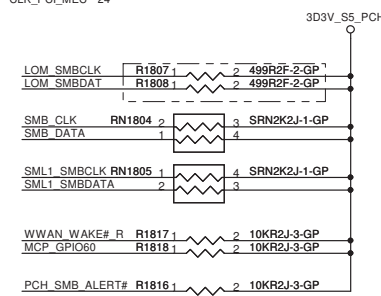
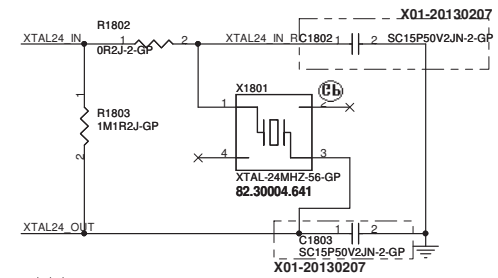
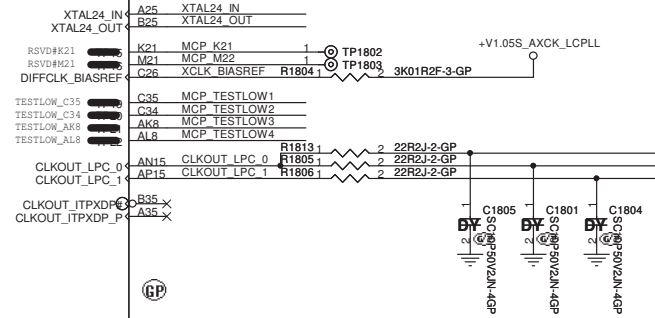
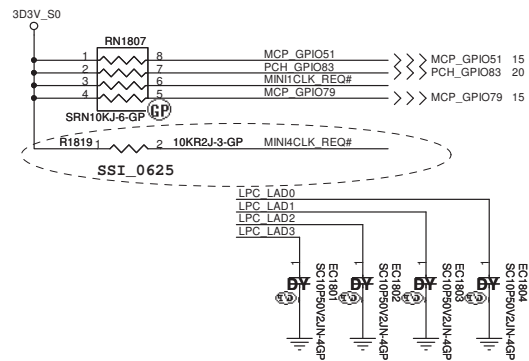
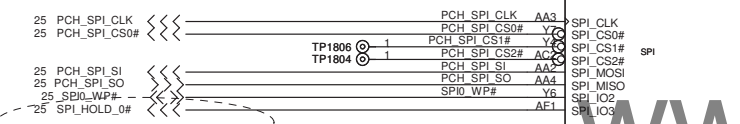
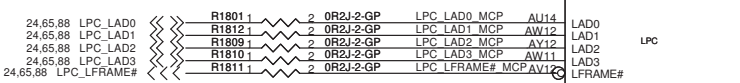
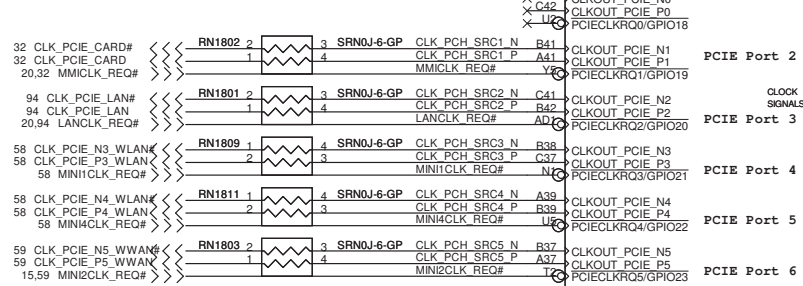
Date: Friday, June 28, 2013

Sheet 17 of 107

SSID = PCH

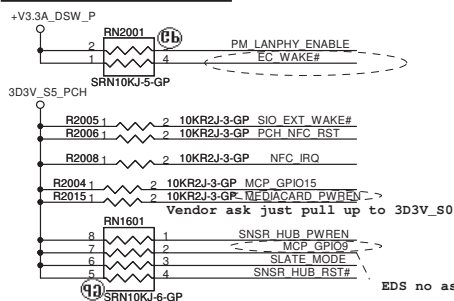
PCIECLKRQ1# and PCIECLKRQ2#  
Support S0 power only

PCIECLKRQn# is route to PCIE Port (n+1)

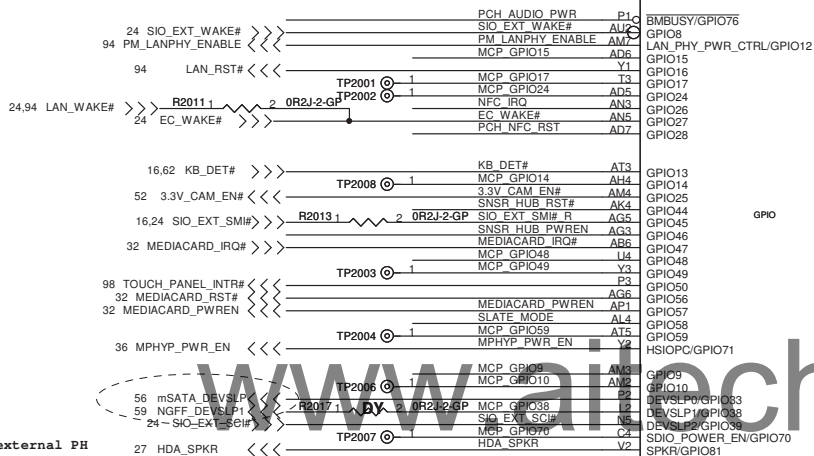
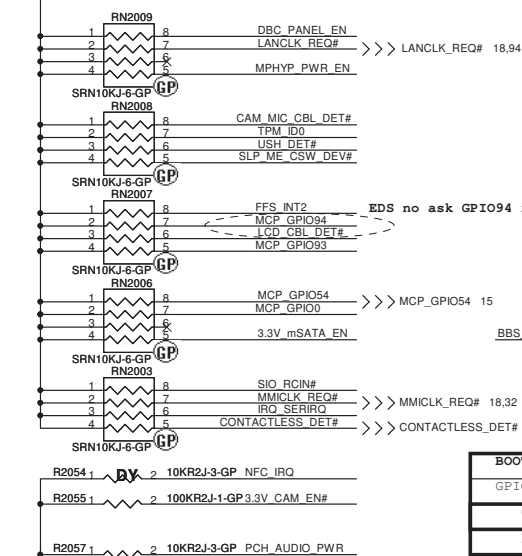
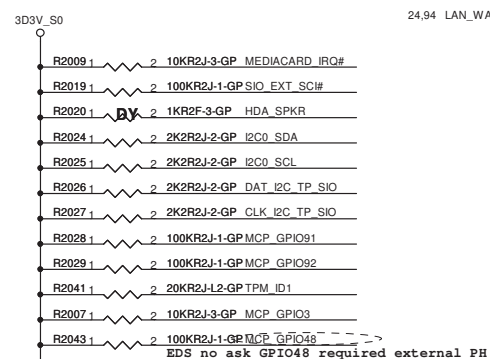




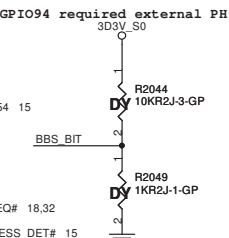
## SSID = PCH



EDS no ask GPIO9 required external PH

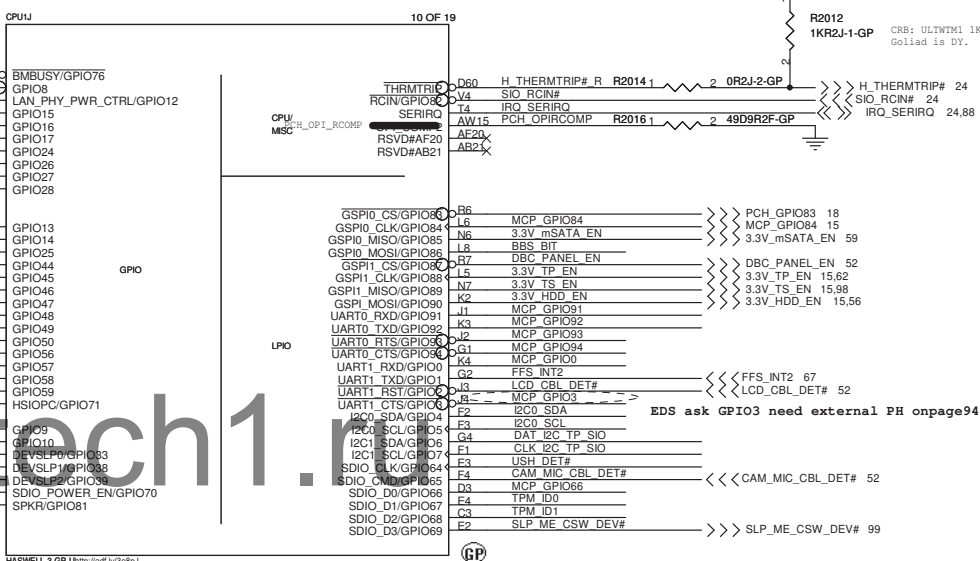


No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot



BOOT BIOS Strap	
GPIO86	BOOT BIOS Location
0	SPI(Default)
1	LPC

TOP-BLOCK SWAP OVERRIDE
GPI066
HIGH pop R20545
LOW pop R2051 (DEFAULT)



&lt;Core Design&gt;



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title
-------

**CPU (GPIO/CPU)**

Size

Document Number

### Round Rock 13.3" UMA

Rev

Date: Friday, June 28, 2013

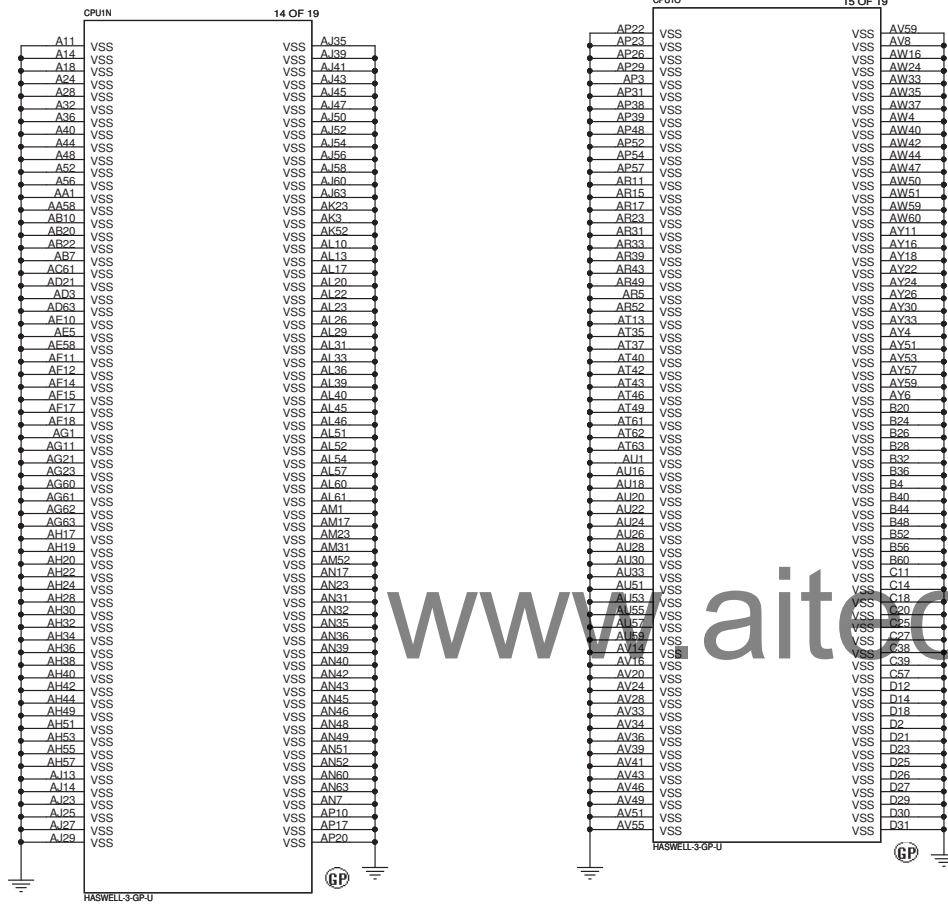
Sheet 20 of 107







SSID = PCH



<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		CPU (VSS)	Rev
Size	Document Number	Round Rock 13.3" UMA	X00
A3			
Date: Friday, June 28, 2013	Sheet	23	of 107

SSID = KBC

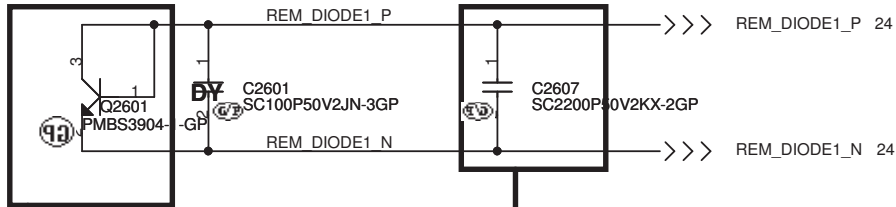
The schematic diagram illustrates the electrical layout of the Dell W1702 UMA board. It features a central U2401 IC (UMA) connected to various peripheral components. Key components include:

- Resistors:** R2401, R2402, R2403, R2404, R2405, R2406, R2407, R2408, R2409, R2410, R2411, R2412, R2413, R2414, R2415, R2416, R2417, R2418, R2419, R2420, R2421, R2422, R2423, R2424, R2425, R2426, R2427, R2428, R2429, R2430, R2431, R2432, R2433, R2434, R2435, R2436, R2437, R2438, R2439, R2440, R2441, R2442, R2443, R2444, R2445, R2446, R2447, R2448, R2449, R2450, R2451, R2452, R2453, R2454, R2455, R2456, R2457, R2458, R2459, R2460, R2461, R2462, R2463, R2464, R2465, R2466, R2467, R2468, R2469, R2470, R2471, R2472, R2473, R2474, R2475, R2476, R2477, R2478, R2479, R2480, R2481, R2482, R2483, R2484, R2485, R2486, R2487, R2488, R2489, R2490, R2491, R2492, R2493, R2494, R2495, R2496, R2497, R2498, R2499, R2500, R2501, R2502, R2503, R2504, R2505, R2506, R2507, R2508, R2509, R2510, R2511, R2512, R2513, R2514, R2515, R2516, R2517, R2518, R2519, R2520, R2521, R2522, R2523, R2524, R2525, R2526, R2527, R2528, R2529, R2530, R2531, R2532, R2533, R2534, R2535, R2536, R2537, R2538, R2539, R2540, R2541, R2542, R2543, R2544, R2545, R2546, R2547, R2548, R2549, R2550, R2551, R2552, R2553, R2554, R2555, R2556, R2557, R2558, R2559, R2560, R2561, R2562, R2563, R2564, R2565, R2566, R2567, R2568, R2569, R2570, R2571, R2572, R2573, R2574, R2575, R2576, R2577, R2578, R2579, R2580, R2581, R2582, R2583, R2584, R2585, R2586, R2587, R2588, R2589, R2590, R2591, R2592, R2593, R2594, R2595, R2596, R2597, R2598, R2599, R2600, R2601, R2602, R2603, R2604, R2605, R2606, R2607, R2608, R2609, R2610, R2611, R2612, R2613, R2614, R2615, R2616, R2617, R2618, R2619, R2620, R2621, R2622, R2623, R2624, R2625, R2626, R2627, R2628, R2629, R2630, R2631, R2632, R2633, R2634, R2635, R2636, R2637, R2638, R2639, R2640, R2641, R2642, R2643, R2644, R2645, R2646, R2647, R2648, R2649, R2650, R2651, R2652, R2653, R2654, R2655, R2656, R2657, R2658, R2659, R2660, R2661, R2662, R2663, R2664, R2665, R2666, R2667, R2668, R2669, R2670, R2671, R2672, R2673, R2674, R2675, R2676, R2677, R2678, R2679, R2680, R2681, R2682, R2683, R2684, R2685, R2686, R2687, R2688, R2689, R2690, R2691, R2692, R2693, R2694, R2695, R2696, R2697, R2698, R2699, R2700, R2701, R2702, R2703, R2704, R2705, R2706, R2707, R2708, R2709, R2710, R2711, R2712, R2713, R2714, R2715, R2716, R2717, R2718, R2719, R2720, R2721, R2722, R2723, R2724, R2725, R2726, R2727, R2728, R2729, R2730, R2731, R2732, R2733, R2734, R2735, R2736, R2737, R2738, R2739, R2740, R2741, R2742, R2743, R2744, R2745, R2746, R2747, R2748, R2749, R2750, R2751, R2752, R2753, R2754, R2755, R2756, R2757, R2758, R2759, R2760, R2761, R2762, R2763, R2764, R2765, R2766, R2767, R2768, R2769, R2770, R2771, R2772, R2773, R2774, R2775, R2776, R2777, R2778, R2779, R2780, R2781, R2782, R2783, R2784, R2785, R2786, R2787, R2788, R2789, R2790, R2791, R2792, R2793, R2794, R2795, R2796, R2797, R2798, R2799, R2800, R2801, R2802, R2803, R2804, R2805, R2806, R2807, R2808, R2809, R2810, R2811, R2812, R2813, R2814, R2815, R2816, R2817, R2818, R2819, R2820, R2821, R2822, R2823, R2824, R2825, R2826, R2827, R2828, R2829, R2830, R2831, R2832, R2833, R2834, R2835, R2836, R2837, R2838, R2839, R2840, R2841, R2842, R2843, R2844, R2845, R2846, R2847, R2848, R2849, R2850, R2851, R2852, R2853, R2854, R2855, R2856, R2857, R2858, R2859, R2860, R2861, R2862, R2863, R2864, R2865, R2866, R2867, R2868, R2869, R2870, R2871, R2872, R2873, R2874, R2875, R2876, R2877, R2878, R2879, R2880, R2881, R2882, R2883, R2884, R2885, R2886, R2887, R2888, R2889, R2890, R2891, R2892, R2893, R2894, R2895, R2896, R2897, R2898, R2899, R2900, R2901, R2902, R2903, R2904, R2905, R2906, R2907, R2908, R2909, R2910, R2911, R2912, R2913, R2914, R2915, R2916, R2917, R2918, R2919, R2920, R2921, R2922, R2923, R2924, R2925, R2926, R2927, R2928, R2929, R2930, R2931, R2932, R2933, R2934, R2935, R2936, R2937, R2938, R2939, R2940, R2941, R2942, R2943, R2944, R2945, R2946, R2947, R2948, R2949, R2950, R2951, R2952, R2953, R2954, R2955, R2956, R2957, R2958, R2959, R2960, R2961, R2962, R2963, R2964, R2965, R2966, R2967, R2968, R2969, R2970, R2971, R2972, R2973, R2974, R2975, R2976, R2977, R2978, R2979, R2980, R2981, R2982, R2983, R2984, R2985, R2986, R2987, R2988, R2989, R2990, R2991, R2992, R2993, R2994, R2995, R2996, R2997, R2998, R2999, R3000, R3001, R3002, R3003, R3004, R3005, R3006, R3007, R3008, R3009, R3010, R3011, R3012, R3013, R3014, R3015, R3016, R3017, R3018, R3019, R3020, R3021, R3022, R3023, R3024, R3025, R3026, R3027, R3028, R3029, R3030, R3031, R3032, R3033, R3034, R3035, R3036, R3037, R3038, R3039, R3040, R3041, R3042, R3043, R3044, R3045, R3046, R3047, R3048, R3049, R3050, R3051, R3052, R3053, R3054, R3055, R3056, R3057, R3058, R3059, R3060, R30



# SSID = Thermal

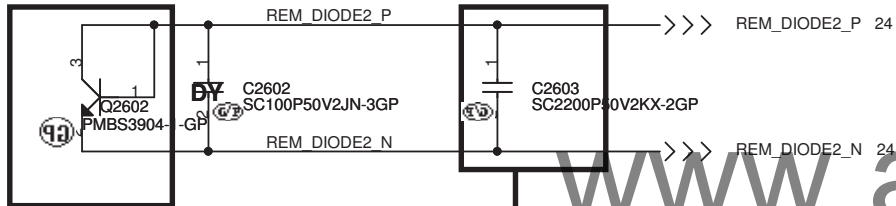
84.03904.L06  
2ND = 84.03904.P11



**Layout Note: Place to CPU**

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

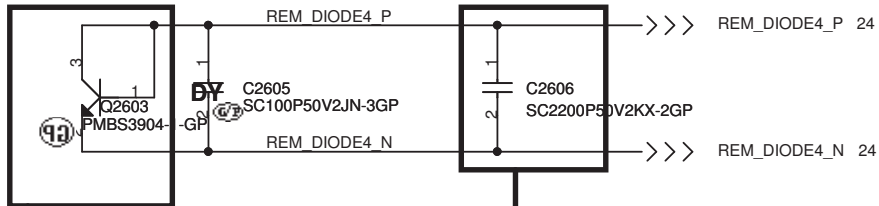
84.03904.L06  
2ND = 84.03904.P11



**Layout Note: Place to DIMM**

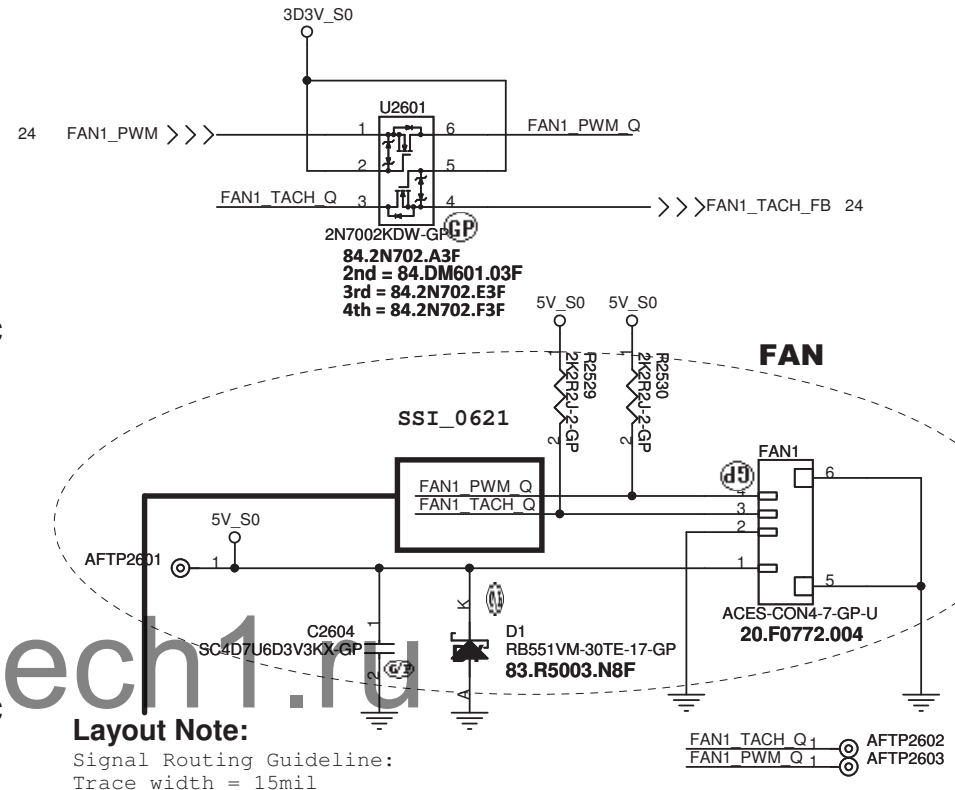
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

84.03904.L06  
2ND = 84.03904.P11



**Layout Note: Place to V.R**

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.



<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title <b>Thermal/Fan</b>		
Size A4	Document Number <b>Round Rock 13.3" UMA</b>	Rev <b>X00</b>
Date: Friday, June 28, 2013	Sheet 26 of 107	



(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***Reserved***

Size  
A

Document Number

***Round Rock 13.3" UMA***

Rev  
***X00***

Date: Friday, June 28, 2013

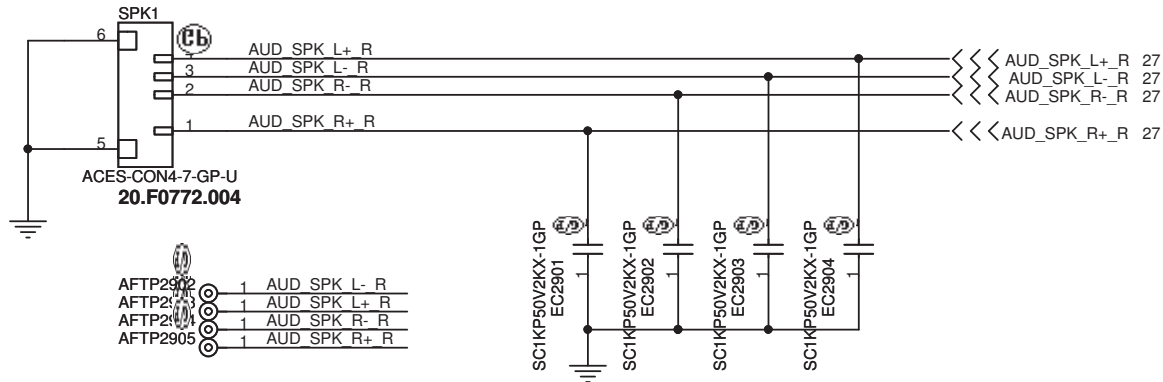
Sheet 28 of 107



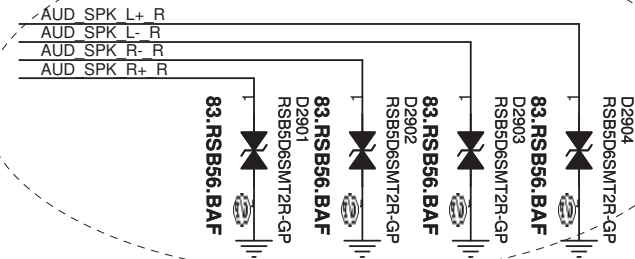
SSID = AUDIO

## Speaker

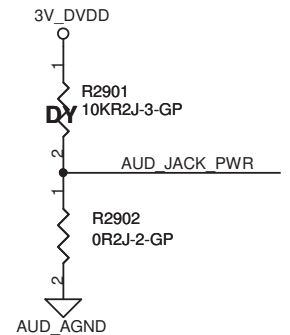
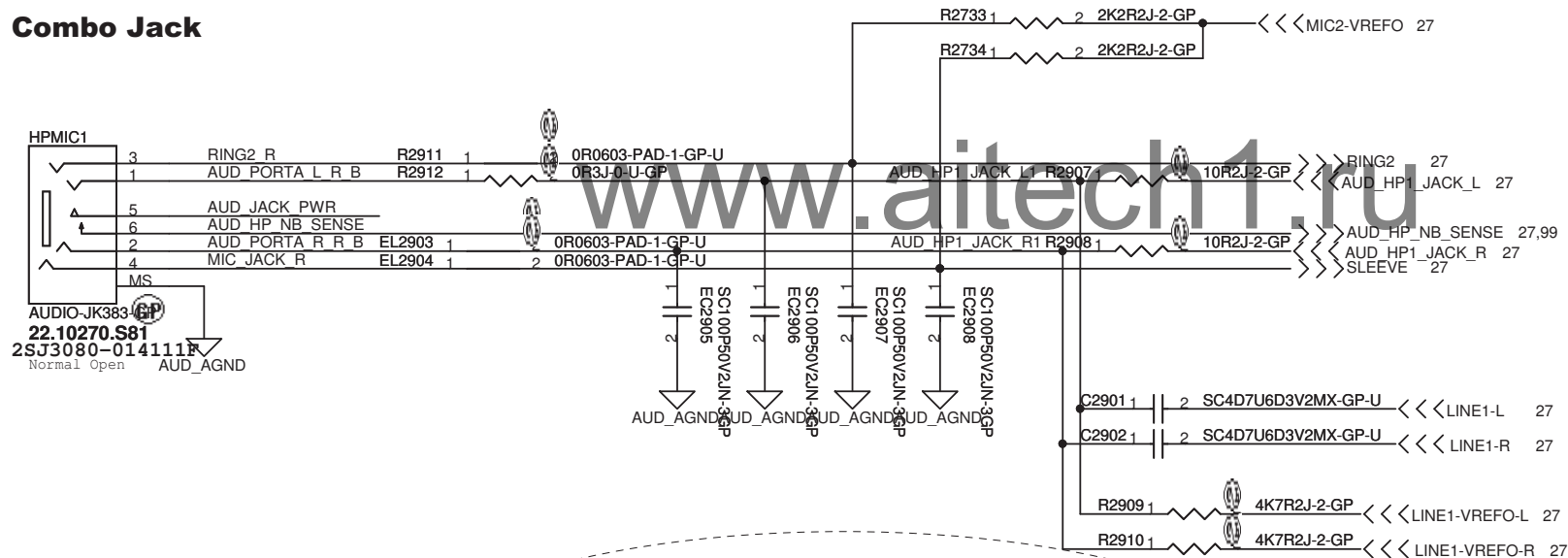
2W/ch



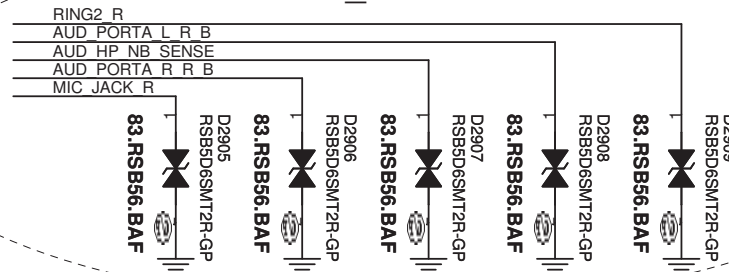
SSI\_0625



## Combo Jack



SSI\_0625



<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Speaker/HPMIC CONN		
Size	Document Number	Rev
A4		X00
Date:	Friday, June 28, 2013	Sheet 29 of 107

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

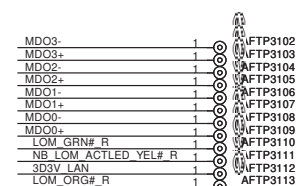
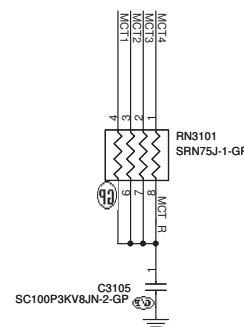
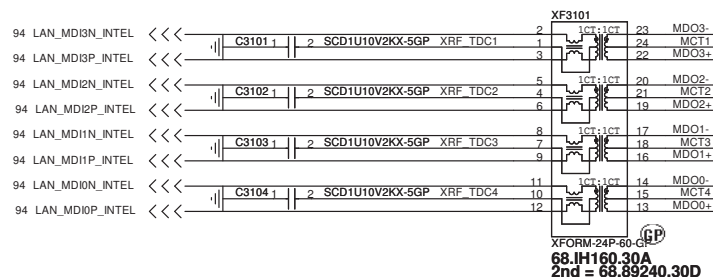
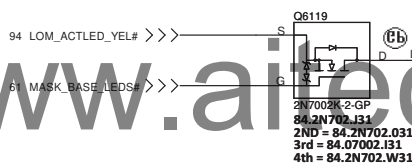
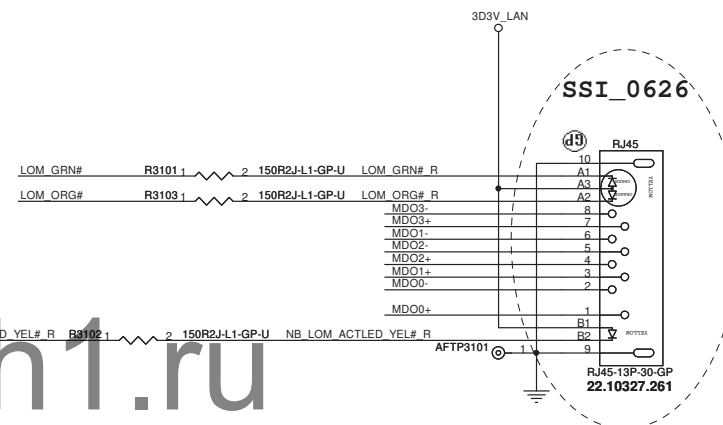
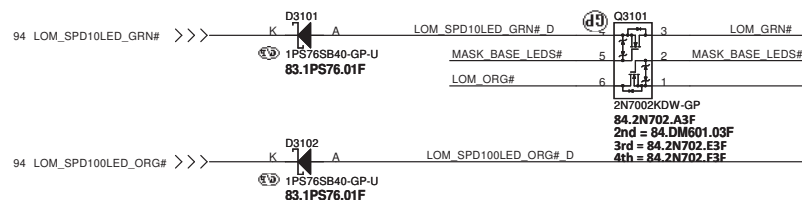
(Blanking)

www.altech1.ru

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <b>Reserved</b>	
Size A	Document Number <b>Round Rock 13.3" UMA</b>		Rev <b>X00</b>
Date: Friday, June 28, 2013		Sheet 30	of 107

SSID = LOM



<Core Design>

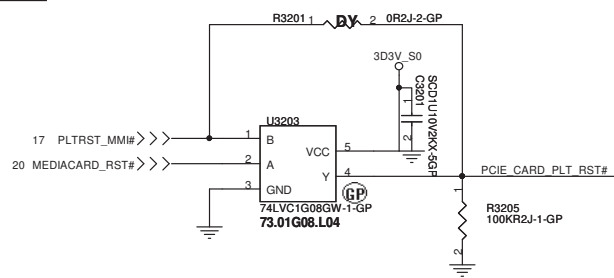
**DELL** Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title **RJ45/Transformer**

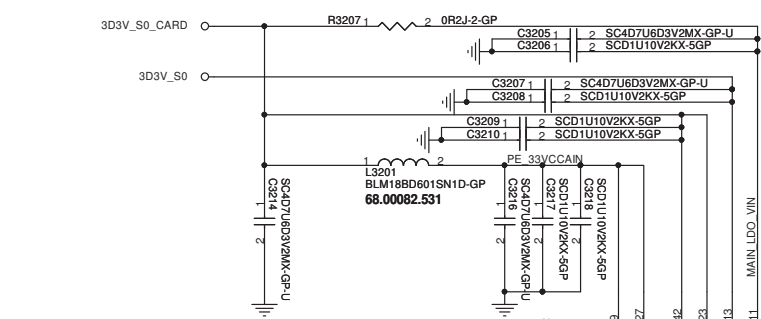
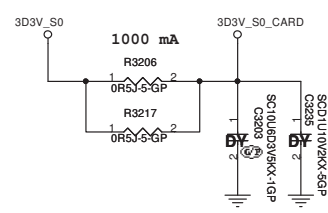
Size A3 Document Number **Round Rock 13.3" UM100** Rev

Date: Friday, June 28, 2013 Sheet 31 of 107

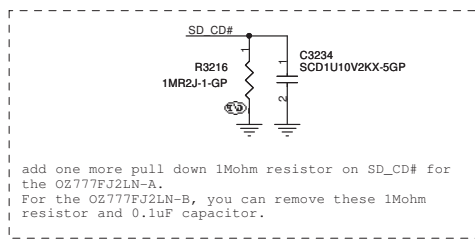
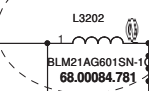
SSID =Card Reader



3D3V\_S0\_CARD



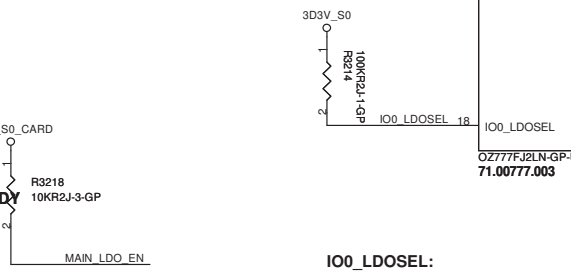
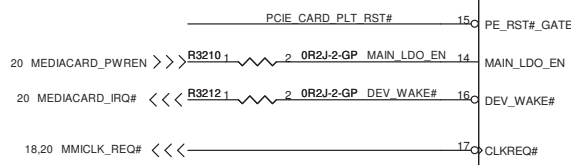
Bead Spec update to 100MHZ/600 ohm/600mA



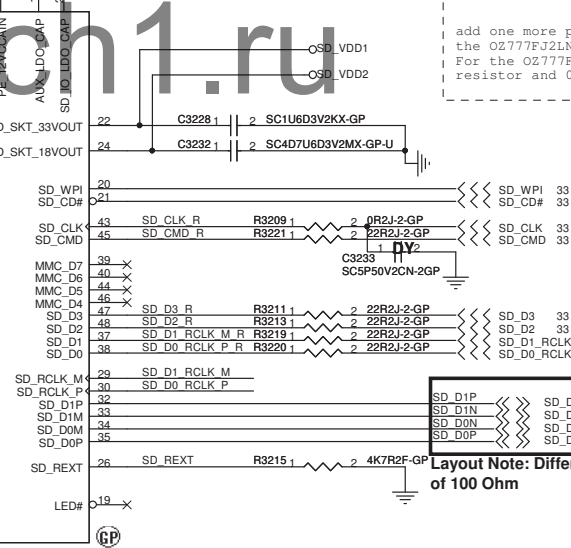
Differential impedance of 85 Ohm

Layout Note:

16	PCIE_TXN2	>>>	16	PCIE_TXN2	>>>
16	PCIE_TXP2	>>>	16	PCIE_TXP2	>>>
16	PCIE_RXP2	<<<	16	PCIE_RXP2	<<<
16	PCIE_RXN2	<<<	16	PCIE_RXN2	<<<
18	CLK_PCIE_CARD#	>>>	18	CLK_PCIE_CARD#	>>>
18	CLK_PCIE_CARD	>>>	18	CLK_PCIE_CARD	>>>



IO0\_LDOSEL:  
High means select internal LDO for main area core power.  
Low means select external LDO for main area core power.



Layout Note: Differential impedance of 100 Ohm

<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

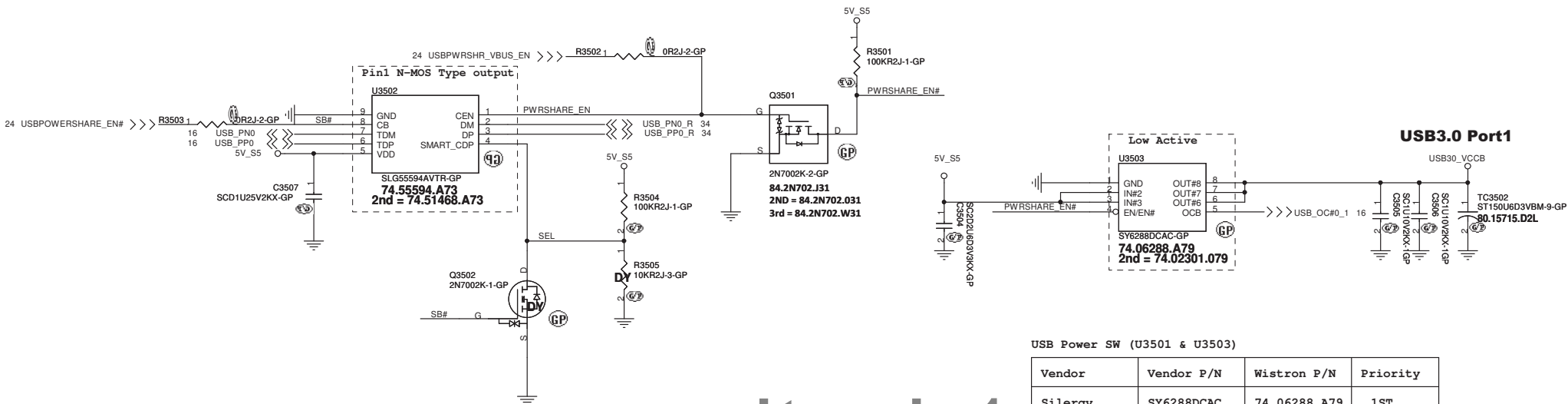
File **Card Reader**

Size A3	Document Number <b>Round Rock 13.3" UMA</b>	Rev <b>X00</b>
Date: Friday, June 28, 2013	Sheet 32	of 107



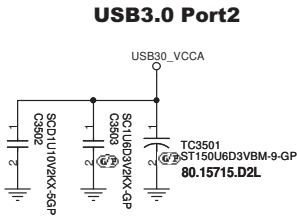
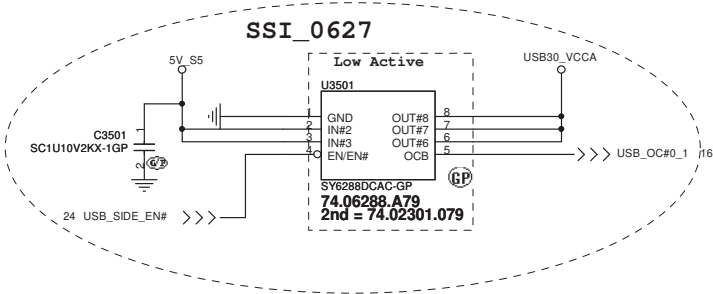


SSID = USB



USB Power SW (U3501 & U3503)

Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DI (Diodes)	AP2301MPG-13	74.02301.079	2ND
			3RD



<Core Design>





SSID = Reset.Suspend

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***S3 Reduction***

Size  
A4

Document Number

***Round Rock 13.3" UMA***

Rev

***X00***

Date: Friday, June 28, 2013

Sheet 37 of 107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A4

Document Number

Rev

**Round Rock 13.3" UMA00**

Date: Friday, June 28, 2013

Sheet 38 of 107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***Reserved***

Size  
A

Document Number

***Round Rock 13.3" UMA***

Rev

***X00***

Date: Friday, June 28, 2013

Sheet 39 of 107

SSID = OBFF

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***Reserved***

Size  
A4

Document Number

***Round Rock 13.3" UMA***

Rev  
***X00***

Date: Friday, June 28, 2013

Sheet 40 of 107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***Reserved***

Size  
A

Document Number

***Round Rock 13.3" UMA***

Rev

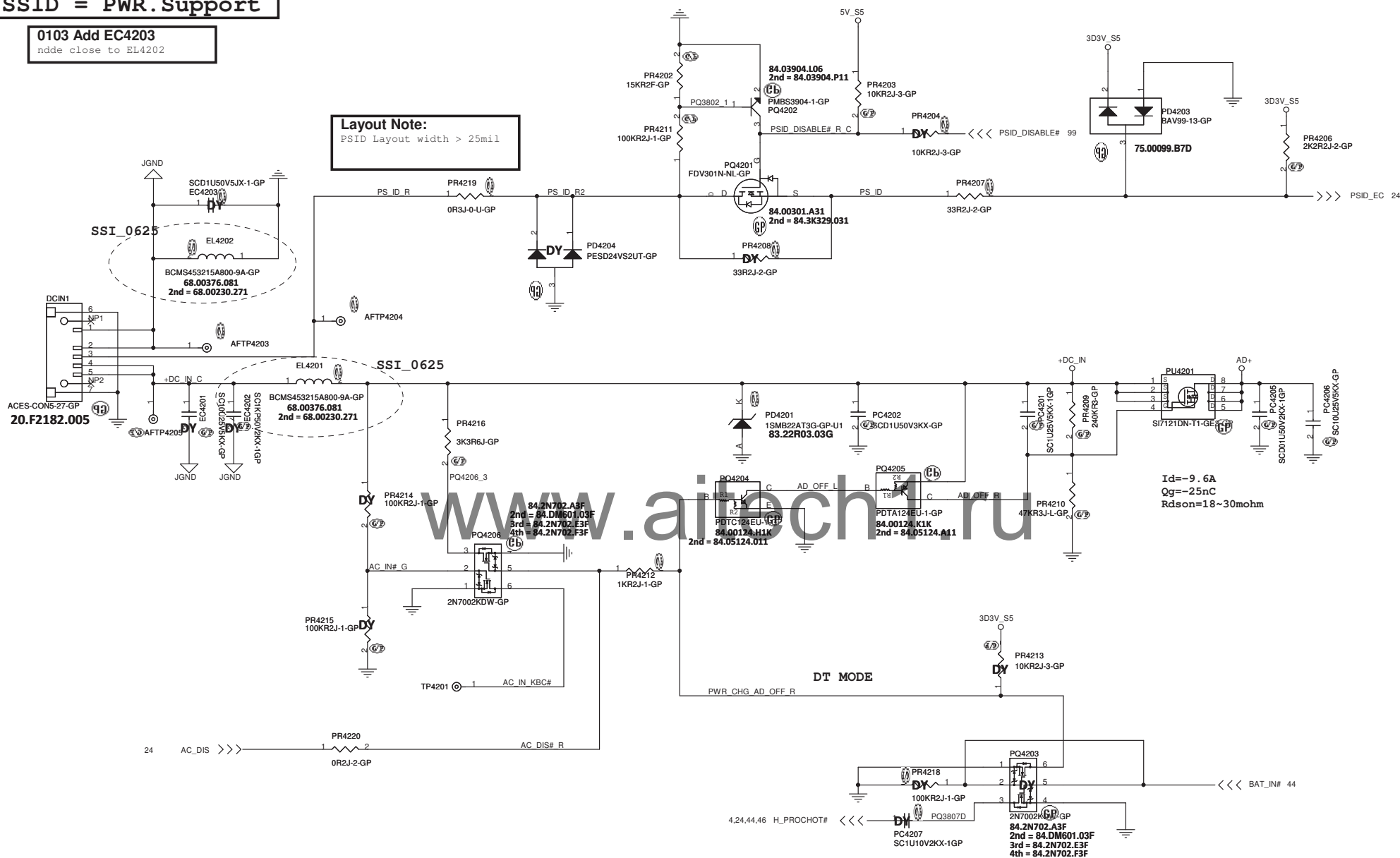
***X00***

Date: Friday, June 28, 2013

Sheet 41 of 107

**0103 Add EC4203**  
ndde close to EL4202

**Layout Note:**  
PSID Layout width > 25mil



<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**DCIN JACK**

Size

Document Number

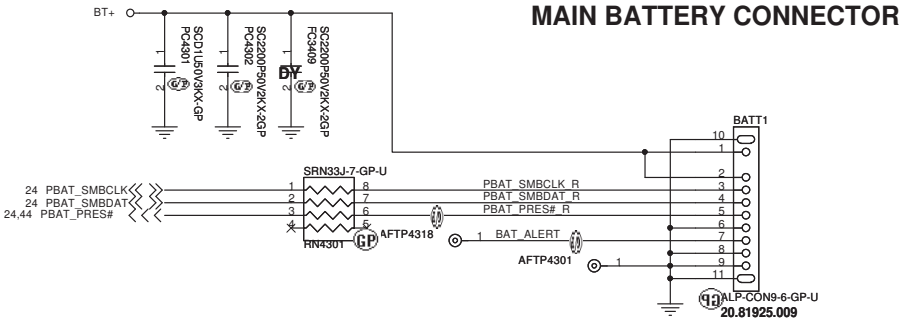
**Round Rock 13.3" UMA**

Rev

Date: Friday, June 28, 2013

Sheet 42 of 107

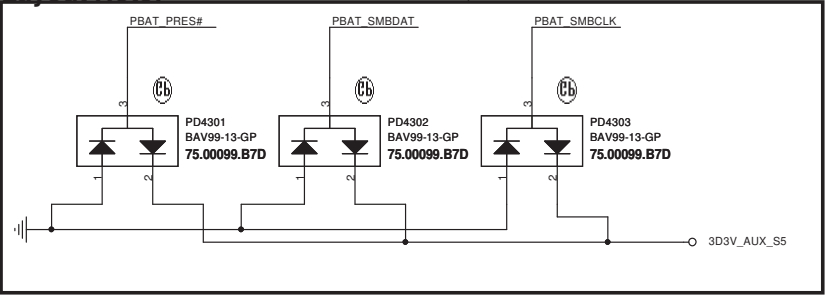
SSID = PWR.Support



www.aitech1.ru

BT- 1 AFTP4302  
PBAT\_SMBCLK R 1 AFTP4303  
PBAT\_SMBDAT R 1 AFTP4304  
PBAT\_PRES# R 1 AFTP4305

Layout Note: Place near Battery CONN



<Core Design>

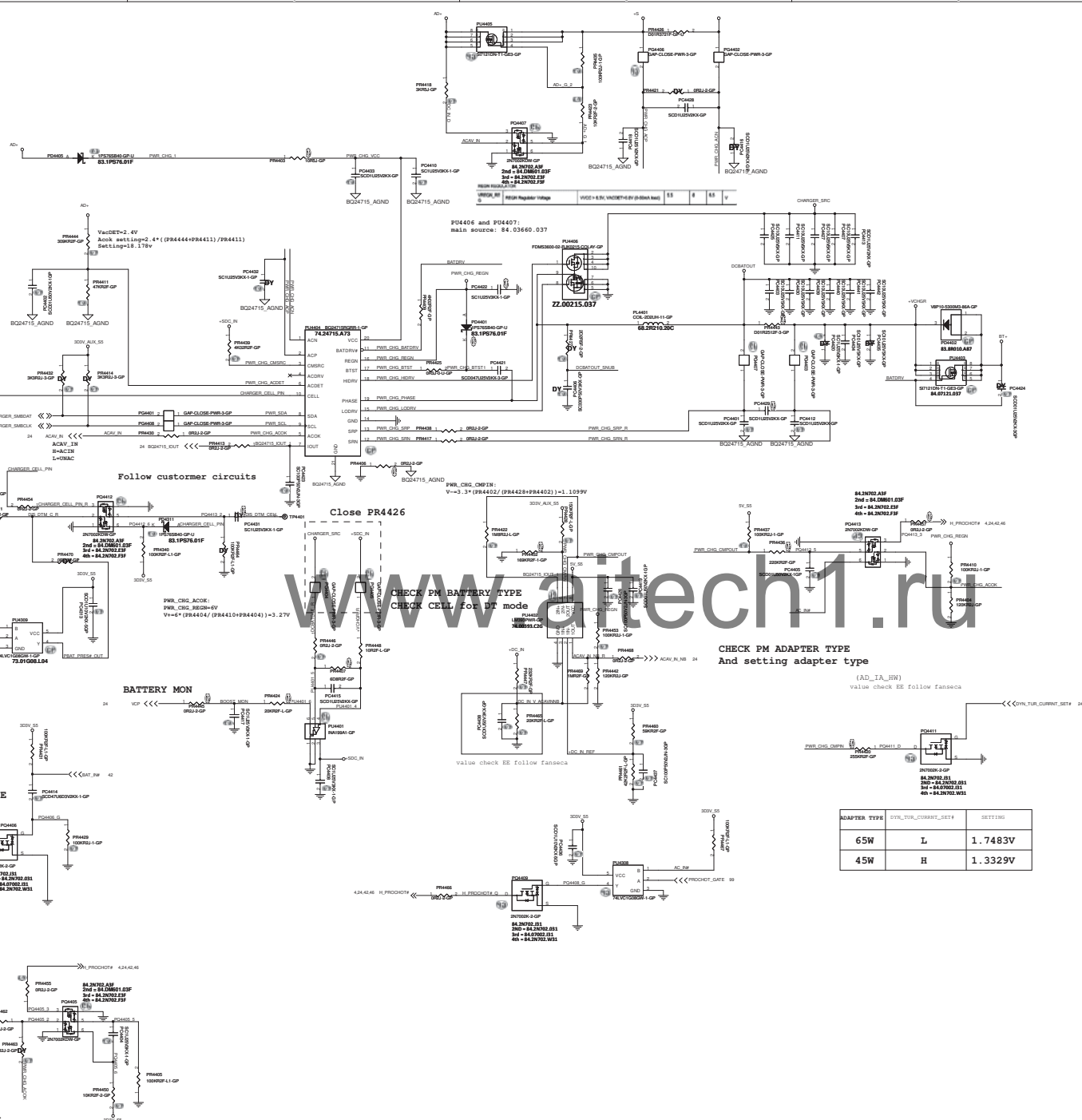
**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File **BATTERY CONN**

Size A3 Document Number **Round Rock 13.3" UMA** Rev **X00**

Date: Friday, June 28, 2013 Sheet 43 of 107

SSID = Charger
----------------

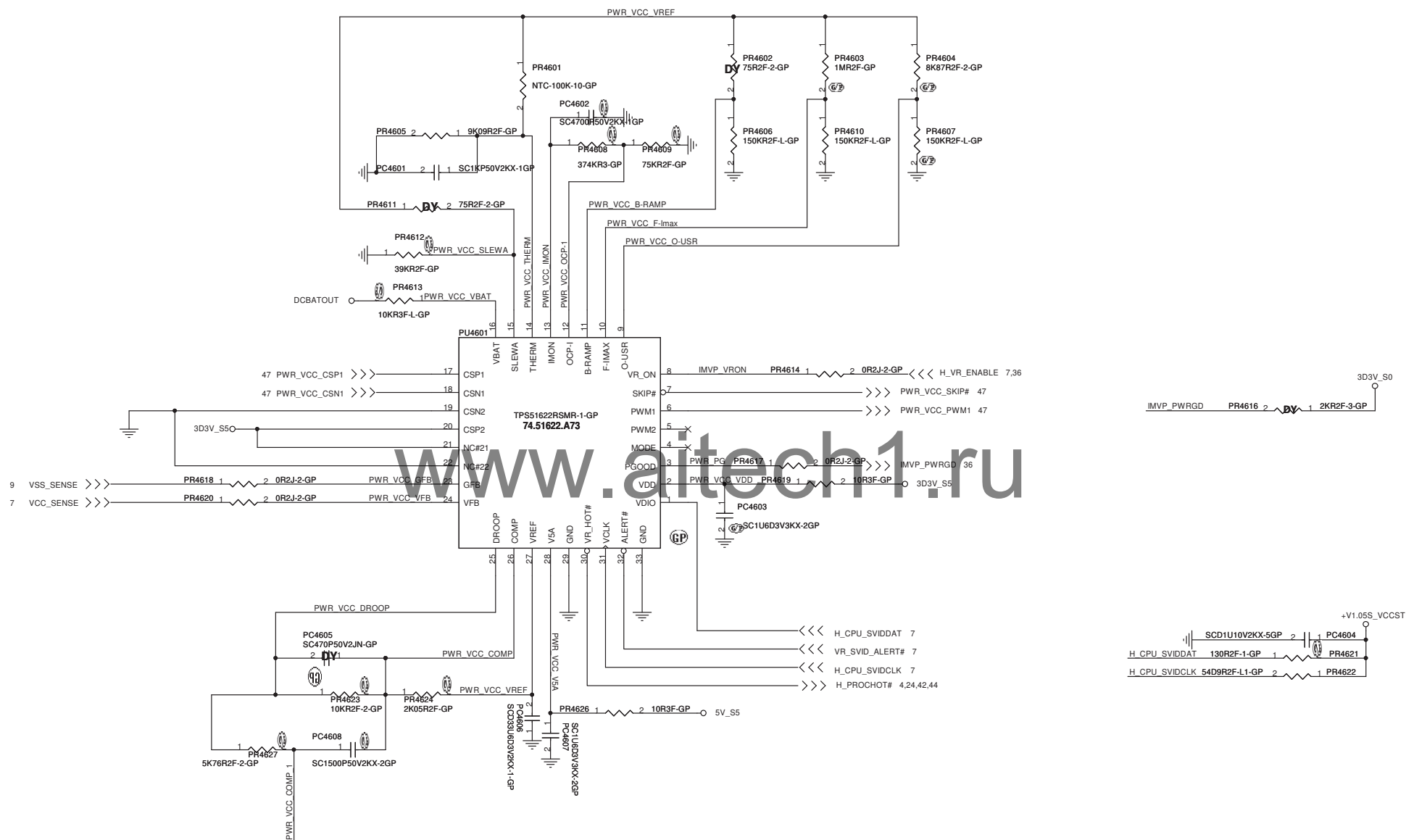


CHECK EE  
follow customer circuits.





```
SSID = CPU.Regulator
```



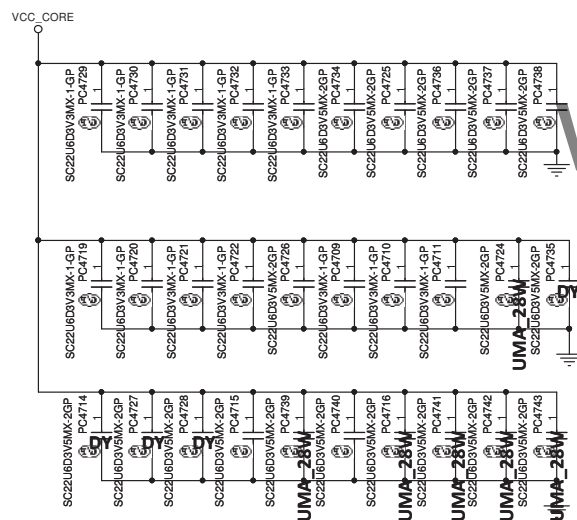
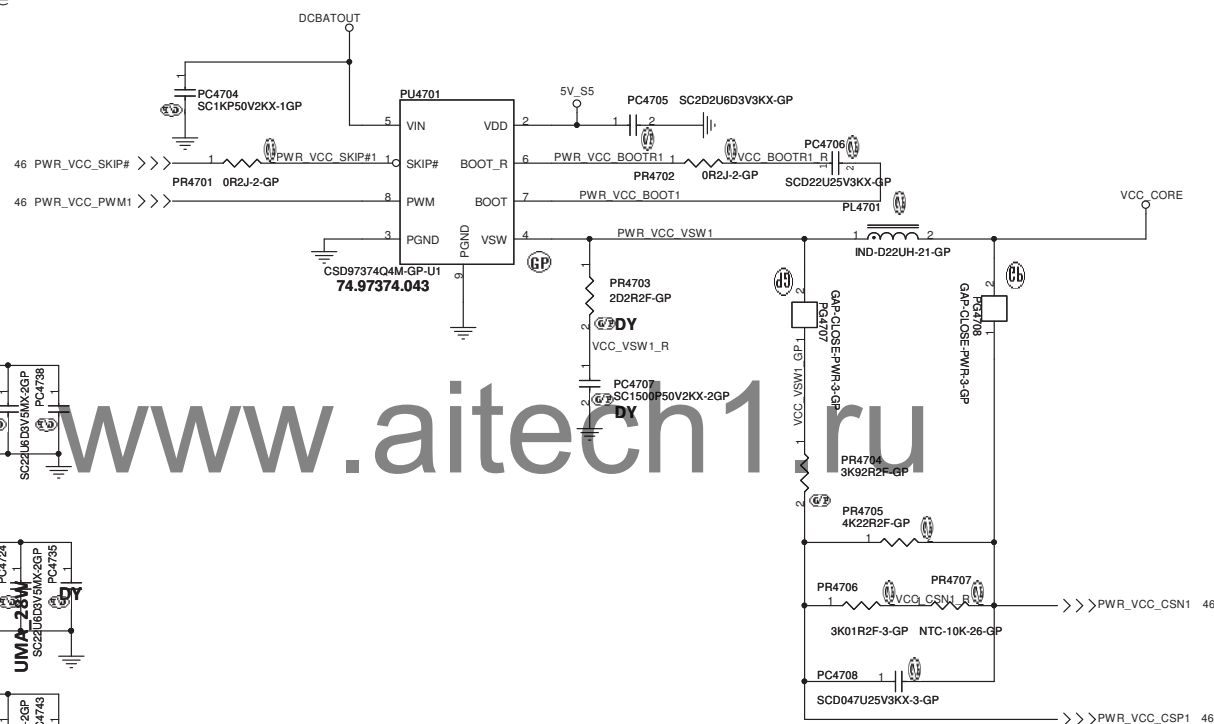
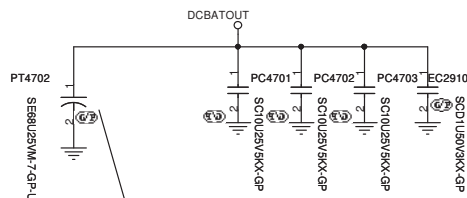
<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>TPS51622 CPUCORE(1/2)</b>			
Size	Document Number		Rev
A3		<b>Round Rock 13.3" UMA</b>	X00
Date:	Friday, June 28, 2013	Sheet 46 of	107

For acoustic noise



DELL

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Size	Document Number
------	-----------------

**Round Rock 13.3" UMA**

Rev	X00
-----	-----

Date: Friday, June 28, 2013

Sheet 47 of 107





(Blanking)

www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***Reserved***

Size  
A4

Document Number

Rev

***Round Rock 13.3" UMA***

Date: Friday, June 28, 2013

Sheet 50 of 107

(Blanking)

[www.aitech1.ru](http://www.aitech1.ru)

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A4

Document Number

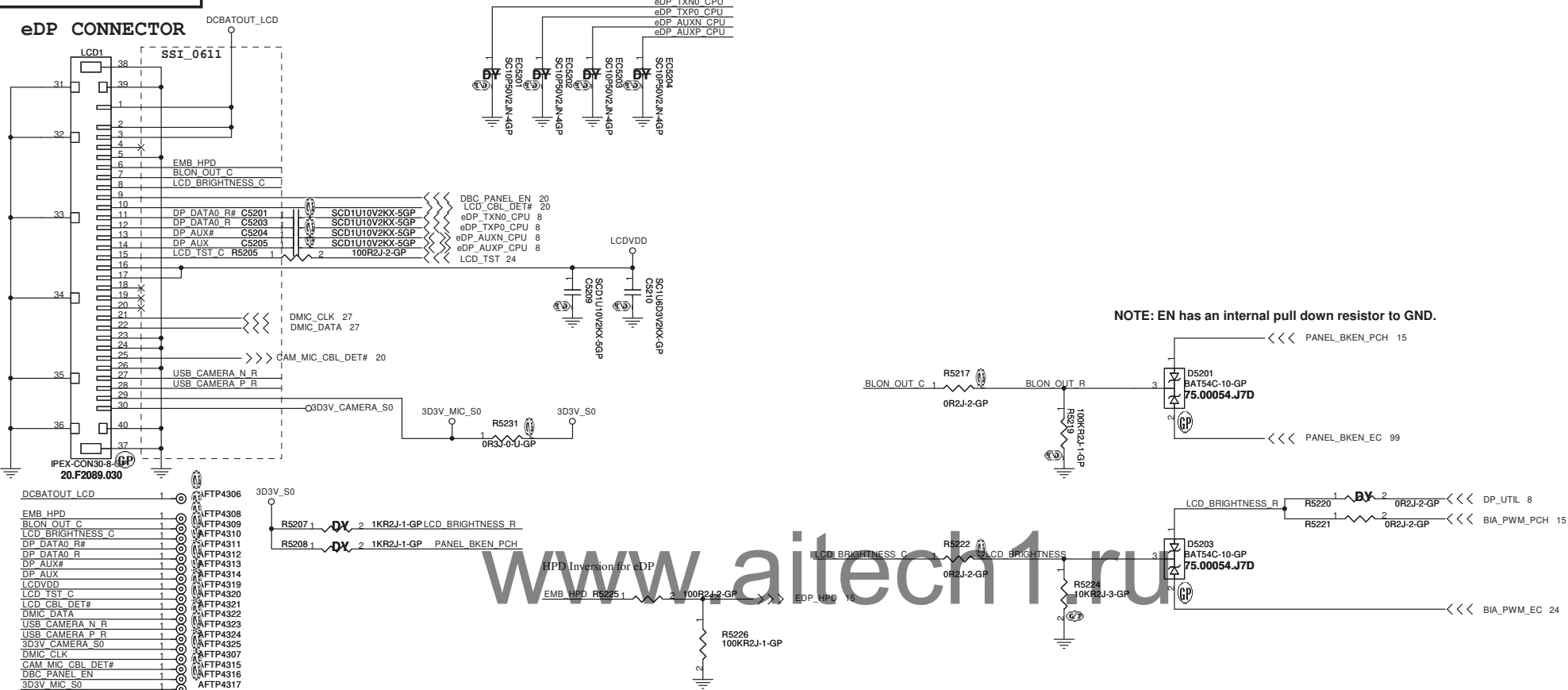
**Round Rock 13.3" UMA**

Rev  
**X00**

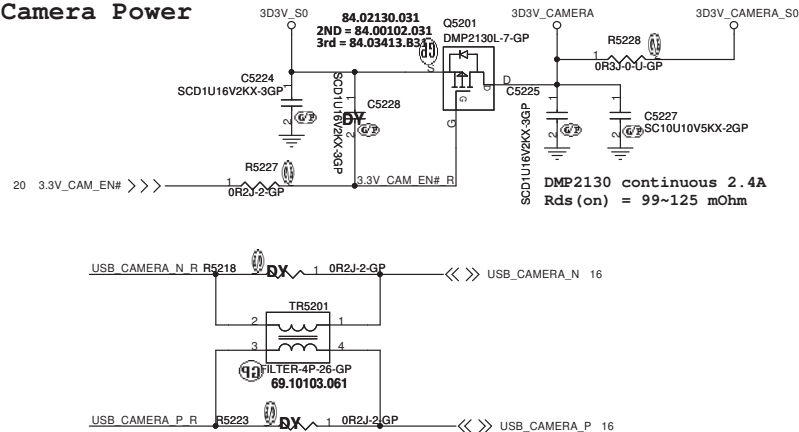
Date: Friday, June 28, 2013

Sheet 51 of 107

## SSID = VIDEO

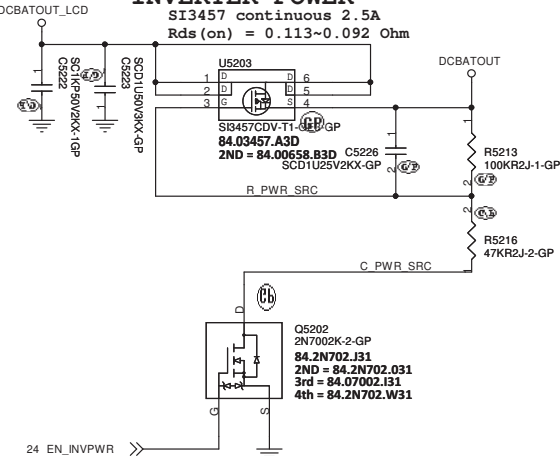


## Camera Power



## INVERTER POWER

SI3457 continuous 2.5A

$$R_{ds(on)} = 0.113 \sim 0.092 \text{ Ohm}$$


## <Core Design>



# Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>eDP Connector</b>			
Size A3	Document Number		Rev
<b>Round Rock 13.3" UMAX00</b>			
Date: Friday, June 28, 2013	Sheet 52	of	107



(Blanking)

www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***Reserved***

Size  
A4

Document Number

***Round Rock 13.3" UMA***

Rev  
X00

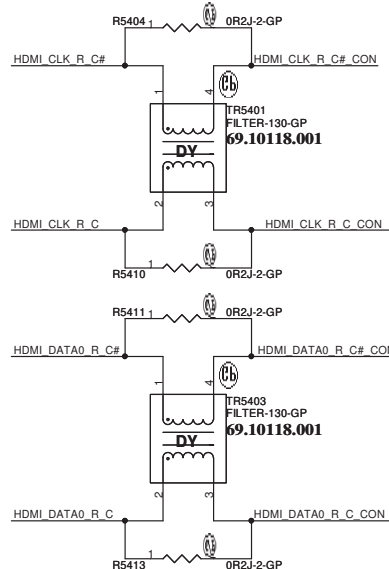
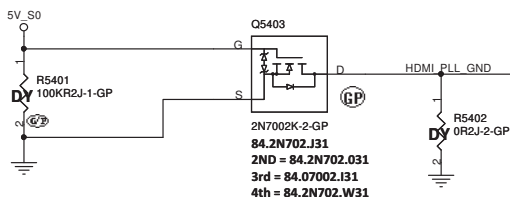
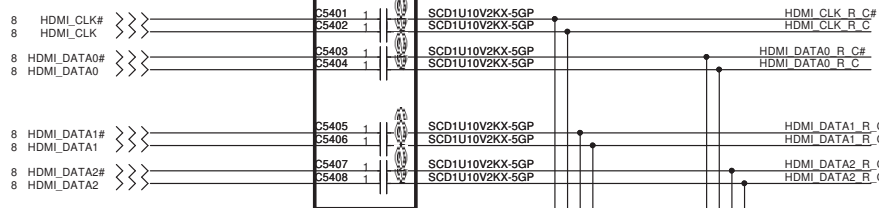
Date: Friday, June 28, 2013

Sheet 53 of 107

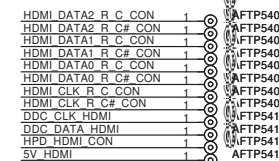
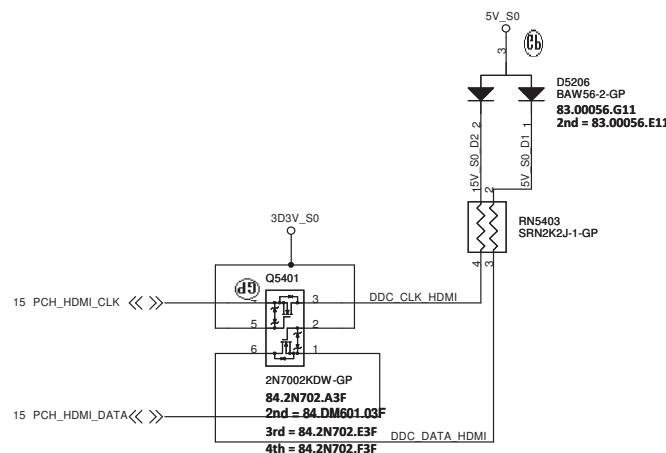
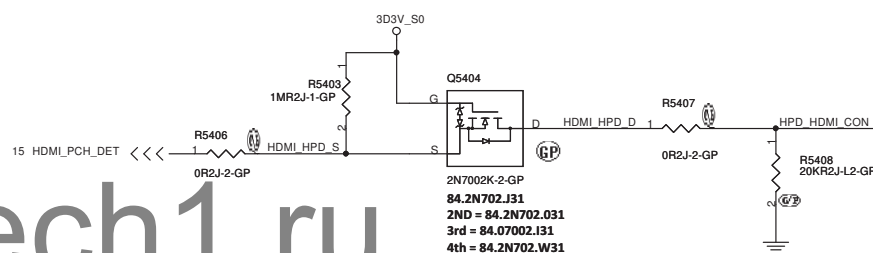
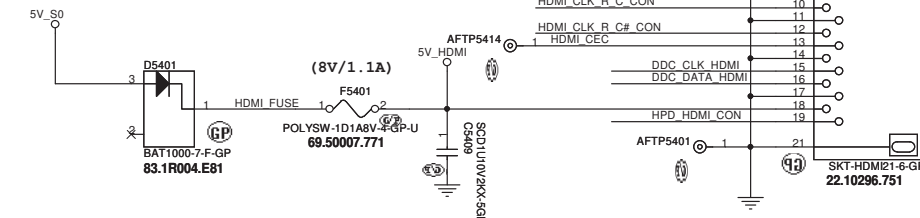
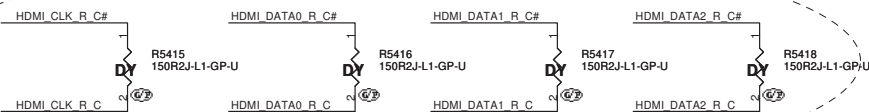
SSID = VIDEO

# HDMI CONNECTOR

Close to HDMI Connector



SSI\_0625



<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **HDMI Level Shifter/Connector**

Size A3 Document Number

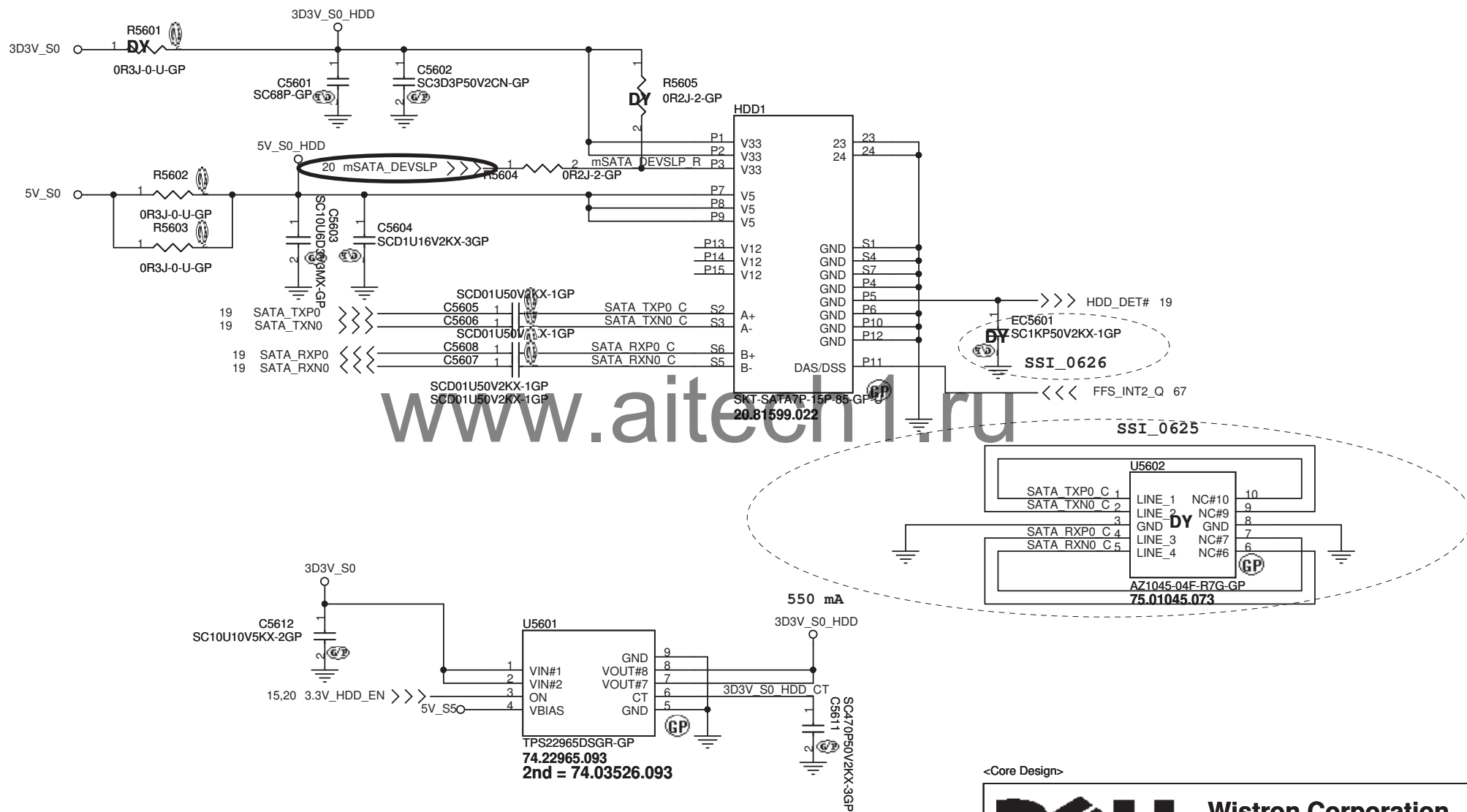
Rev Round Rock 13.3" UMAX00

Date: Friday, June 28, 2013

Sheet 54 of 107



SSID = SATA



<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>HDD</b>			
Size A4	Document Number		Rev X00
		<b>Round Rock 13.3" UMA</b>	
Date: Friday, June 28, 2013		Sheet 56 of	107

(Blanking)

www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***Reserved***

Size  
A4

Document Number

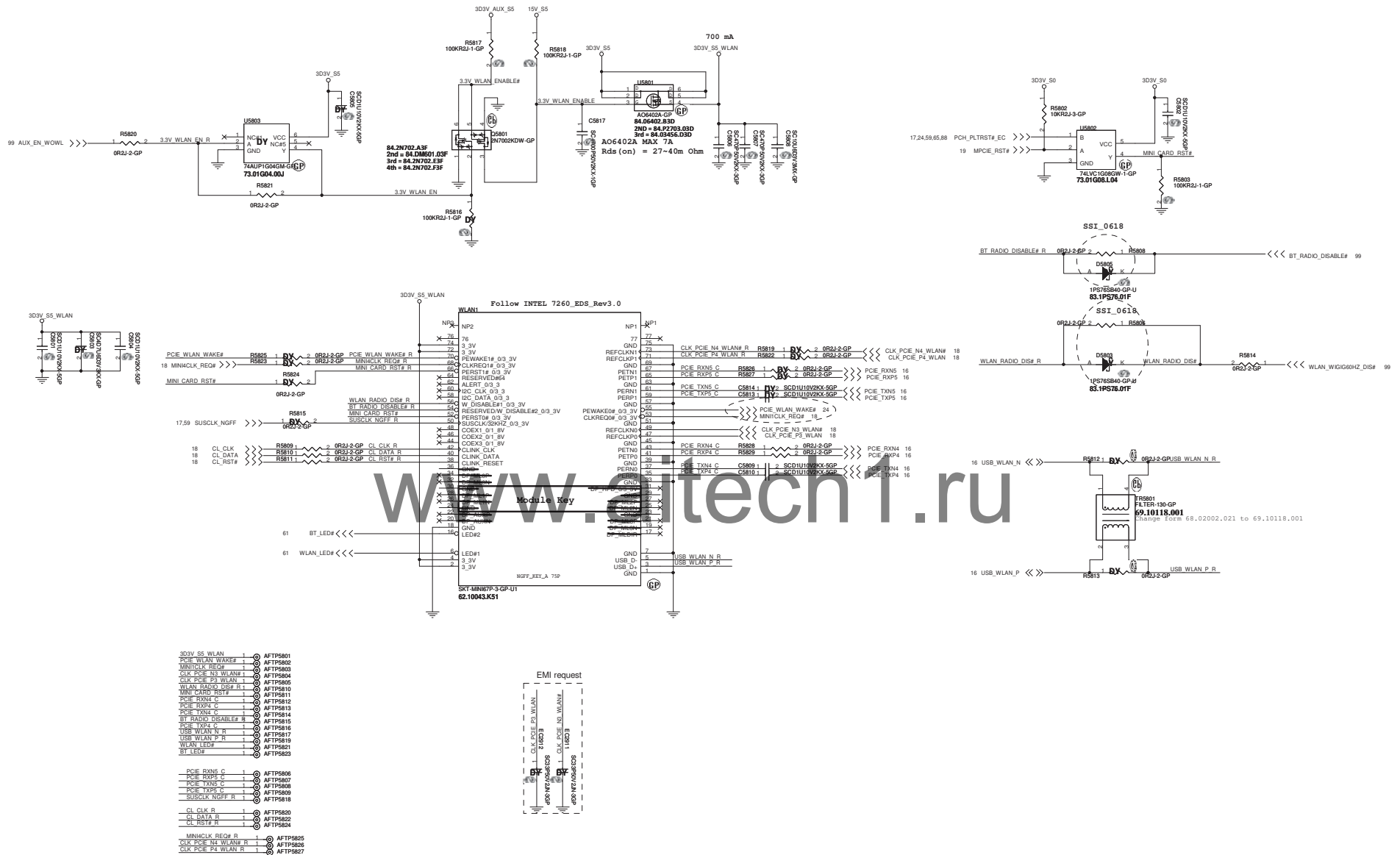
***Round Rock 13.3" UMA***

Rev  
***X00***

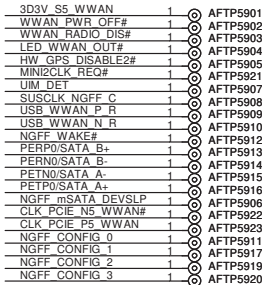
Date: Friday, June 28, 2013

Sheet 57 of 107

## SSID = WIRELESS



**SSID = WIRELESS**



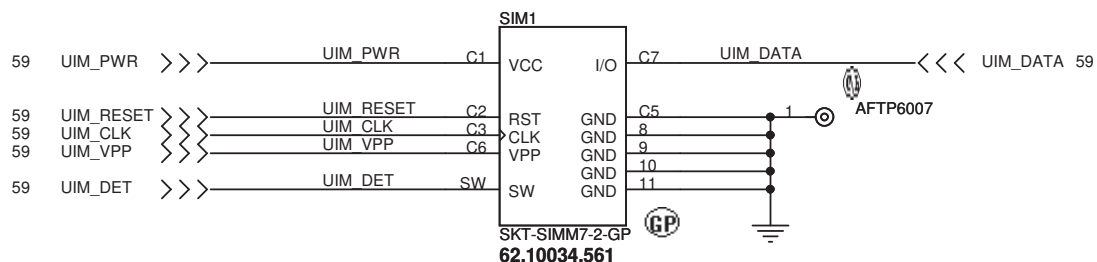
16 USB\_WWAN\_N << >> R5916 1 0P2J2-GP USB\_WWAN\_N R

TR5901  
FILTER-130-GP  
**69.10118.001**  
Change form 68.02002.021 to 69.10118.

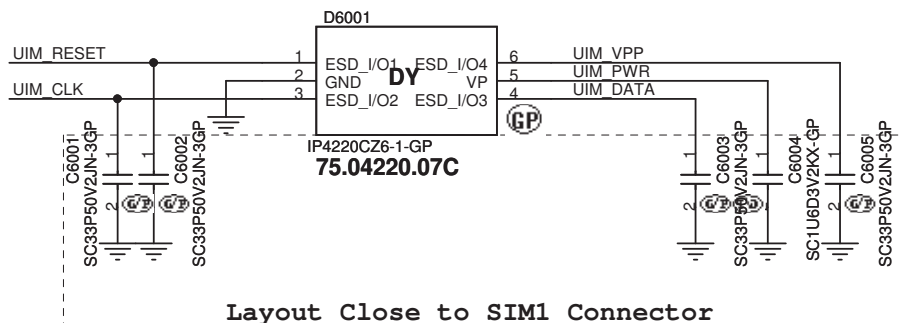
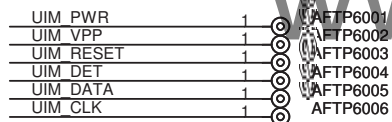
16 USB\_WWAN\_P << >> R5921 1 0P2J2-GP USB\_WWAN\_P R

Title			
<b>NGFF-WWAN/SSD</b>			
Size	Document Number		Rev
	<b>Round Rock 13.3" UMA</b>		<b>X</b>
Date:	Friday, June 28, 2013	Sheet	59 of 107

SSID =WIRELESS



PIN	62.10034.561 Micro SIM PinDefine
C1	VCC
C2	RST
C3	CLK
C4	Reserve
C5	GND
C6	VPP
C7	I/O
SW	SIM Card Detect
8	PTH GND
9	PTH GND
10	PTH GND
11	PTH GND



Layout Close to SIM1 Connector

<Core Design>



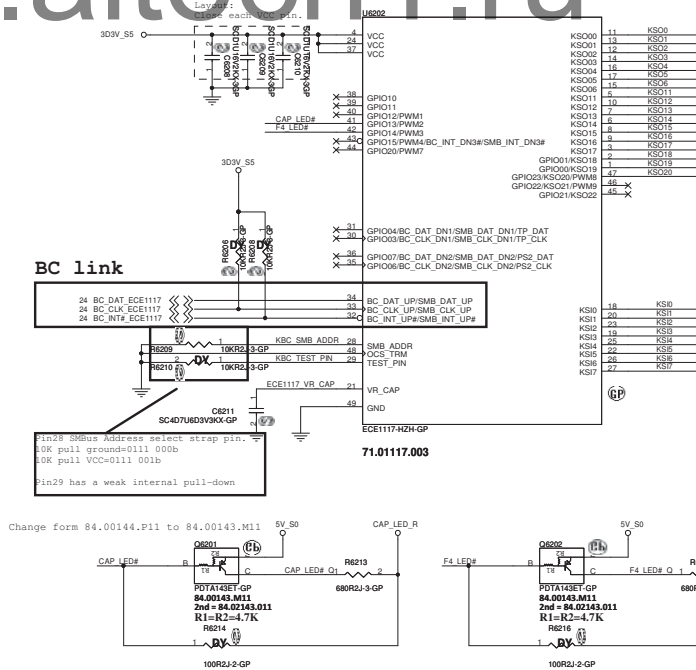
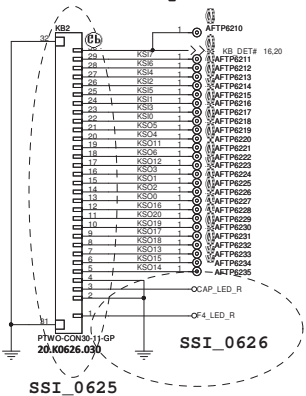
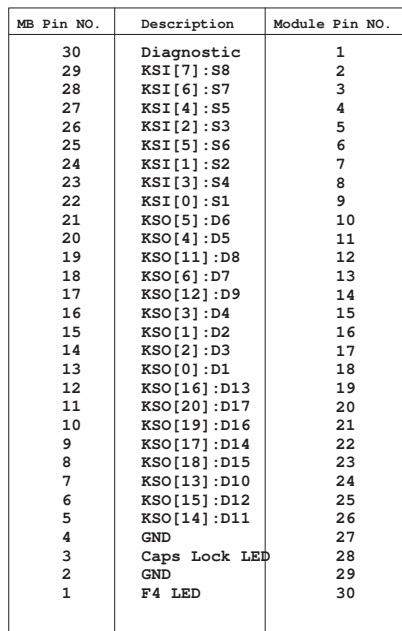
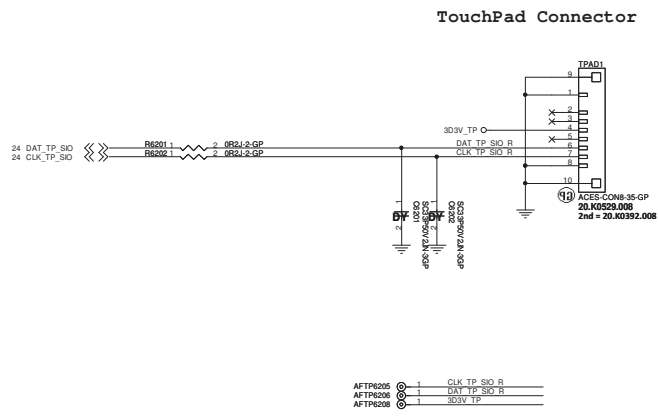
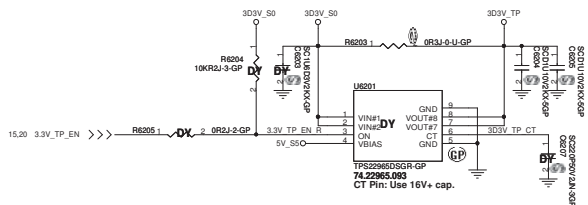
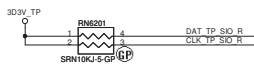
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title				
<b>mSATA</b>				
Size	Document Number			Rev
<b>Round Rock 13.3" UMA</b>			<b>X000</b>	
Date:	Friday, June 28, 2013		Sheet 60 of	107





SSID = KBC	SSID = Touch.Pad
------------	------------------



&lt;Core Design&gt;

**DELL** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>Key Board/Touch Pad</b>
-------	----------------------------

Size	Document Number
	<b>Round Rock 13.3" UMA</b>

Date: Friday, June 28, 2013 Sheet 62 of 107

(Blanking)

www.aitech1.ru

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**IO CONN**

Size  
A4

Document Number

**Round Rock 13.3" UMA**

Rev  
**X00**

Date: Friday, June 28, 2013

Sheet 63 of 107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Hall Sensor**

Size

Document Number

**Round Rock 13.3" UMA**

Rev

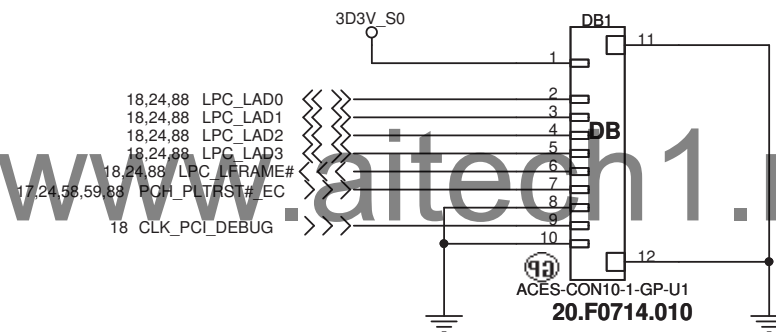
**X00**

Date: Friday, June 28, 2013

Sheet 64 of 107

SSID = DEBUG PORT

SB modify to test pad



<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Debug connector**

Size

Document Number

**Round Rock 13.3" UMA**

Rev

**X00**

Date: Friday, June 28, 2013

Sheet 65 of 107

www.aitech1.ru

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**SENSOR**

Size  
A3

Document Number

**Round Rock 13.3" UMA**

Rev

**X00**

Date: Friday, June 28, 2013

Sheet 66 of 107



(Blanking)

www.aitech1.ru

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Thunderbolt (1/5)**

Size  
A3

Document Number

**Round Rock 13.3" UMA**

Rev  
**X00**

Date: Friday, June 28, 2013

Sheet 68 of 107



(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***Thunderbolt (2/5)***

Size  
A

Document Number

***Round Rock 13.3" UMA***

Rev

***X00***

Date: Friday, June 28, 2013

Sheet 69 of 107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***Thunderbolt (3/5)***

Size  
A

Document Number

***Round Rock 13.3" UMA***

Rev

***X00***

Date: Friday, June 28, 2013

Sheet 70 of 107

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

(Blanking)

www.altech1.ru

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b><i>Thunderbolt (4/5)</i></b>			
Size A	Document Number <b><i>Round Rock 13.3" UMA</i></b>		Rev <b><i>X00</i></b>
Date:	Friday, June 28, 2013	Sheet 71 of	107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***Thunderbolt (5/5)***

Size  
A

Document Number

***Round Rock 13.3" UMA***

Rev

***X00***

Date: Friday, June 28, 2013

Sheet 72 of 107

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

(Blanking)

www.altech1.ru

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b><i>GPU (1/5) PEG</i></b>			
Size A	Document Number <b><i>Round Rock 13.3" UMA</i></b>		Rev <b><i>X00</i></b>
Date:	Friday, June 28, 2013	Sheet 73 of	107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***GPU (2/5) DIGITAL***

Size  
A

Document Number

***Round Rock 13.3" UMA***

Rev

***X00***

Date: Friday, June 28, 2013

Sheet 74 of 107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**GPU (3/5) VRAM**

Size  
A

Document Number

**Round Rock 13.3" UMA**

Rev

**X00**

Date: Friday, June 28, 2013

Sheet 75 of 107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**GPU (4/5) GPIO**

Size  
A

Document Number

**Round Rock 13.3" UMA**

Rev

**X00**

Date: Friday, June 28, 2013

Sheet 76 of 107



	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

(Blanking)

www.aitech1.ru

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b><i>GPU (5/5) PWR/GND</i></b>			
Size A	Document Number <b><i>Round Rock 13.3" UMA</i></b>		Rev <b><i>X00</i></b>
Date:	Friday, June 28, 2013	Sheet 77 of	107



(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**VRAM3,4 (2/4)**

Size  
A

Document Number

**Round Rock 13.3" UMA**

Rev

**X00**

Date: Friday, June 28, 2013

Sheet 79 of 107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**VRAM5,6 (3/4)**

Size  
A

Document Number

**Round Rock 13.3" UMA**

Rev

**X00**

Date: Friday, June 28, 2013

Sheet 80 of 107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**VRAM7,8 (4/4)**

Size  
A

Document Number

**Round Rock 13.3" UMA**

Rev

**X00**

Date: Friday, June 28, 2013

Sheet 81 of 107



	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

(Blanking)

www.altech1.ru

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <b>DISCRETE VGAPOWER</b>	
Size A	Document Number <b>Round Rock 13.3" UMA</b>		Rev <b>X00</b>
Date: Friday, June 28, 2013		Sheet 83 of	107

(Blanking)

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Switchable GFXLCD**

Size  
A

Document Number

**Round Rock 13.3" UMA**

Rev

**X00**

Date: Friday, June 28, 2013

Sheet 84 of 107



(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Switchable GFXCRT**

Size  
A

Document Number

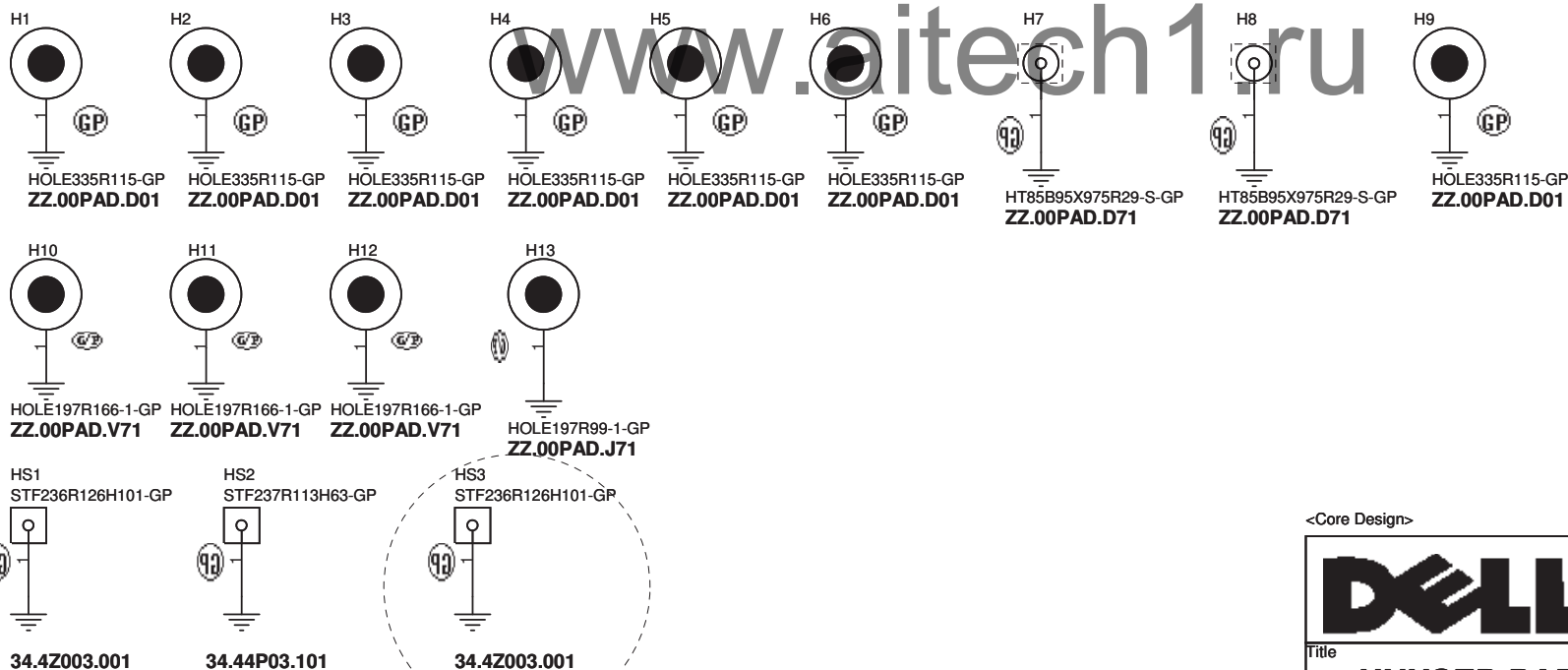
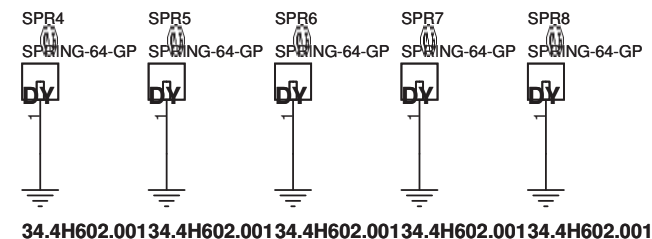
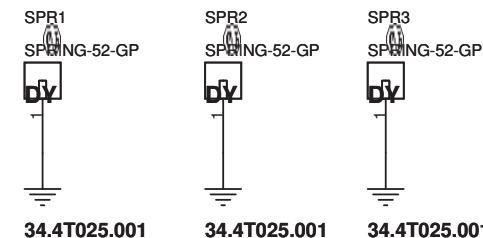
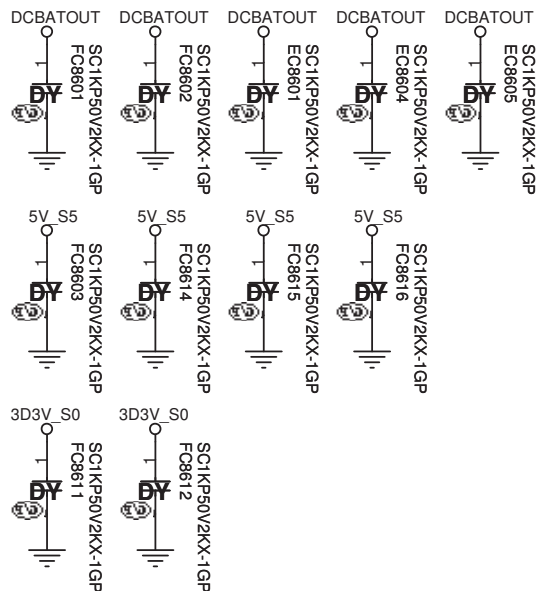
**Round Rock 13.3" UMA**

Rev

**X00**

Date: Friday, June 28, 2013

Sheet 85 of 107



<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		Rev
UNUSED PARTS/EMI Capacitors		X00
Size	Document Number	
Round Rock 13.3" UMA		
Date: Friday, June 28, 2013	Sheet 86 of 107	

SSID = USH

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***USH Board Connector***

Size  
A4

Document Number

**Round Rock 13.3" UMA**

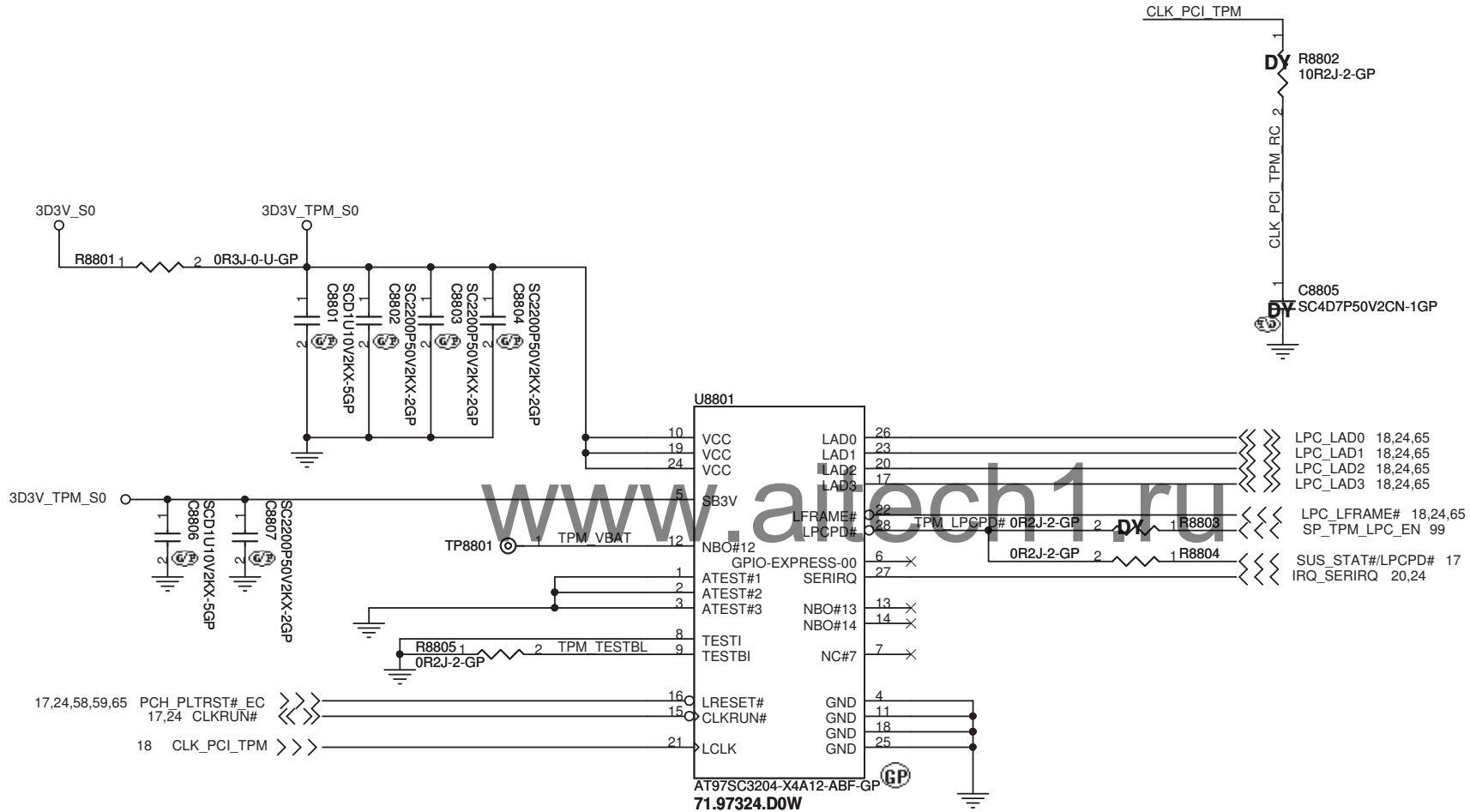
Rev  
**X00**

Date: Friday, June 28, 2013

Sheet 87 of 107

SSID = TPM

Place close to Pin 21



<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**TPM**

Size

Document Number

**Round Rock 13.3" UMA**

Rev

**X00**

Date: Friday, June 28, 2013

Sheet 88 of 107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***Finger Print***

Size  
A

Document Number

***Round Rock 13.3" UMA***

Rev

***X00***

Date: Friday, June 28, 2013

Sheet 89 of 107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

***NFC Connector***

Size  
A4

Document Number

***Round Rock 13.3" UMA***

Rev

***X00***

Date: Friday, June 28, 2013

Sheet 90 of 107

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Smart Card**

Size

Document Number

Rev

**Round Rock 13.3" UMA**

**X00**

Date: Friday, June 28, 2013

Sheet 91 of 107

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

(Blanking)

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b><i>Reserved</i></b>			
Size A	Document Number <b><i>Round Rock 13.3" UMA</i></b>		Rev <b><i>X00</i></b>
Date:	Friday, June 28, 2013	Sheet 92 of	107



SSID = Docking

(Blanking)  
www.aitech1.ru

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**DOCKING**

Size  
A4

Document Number

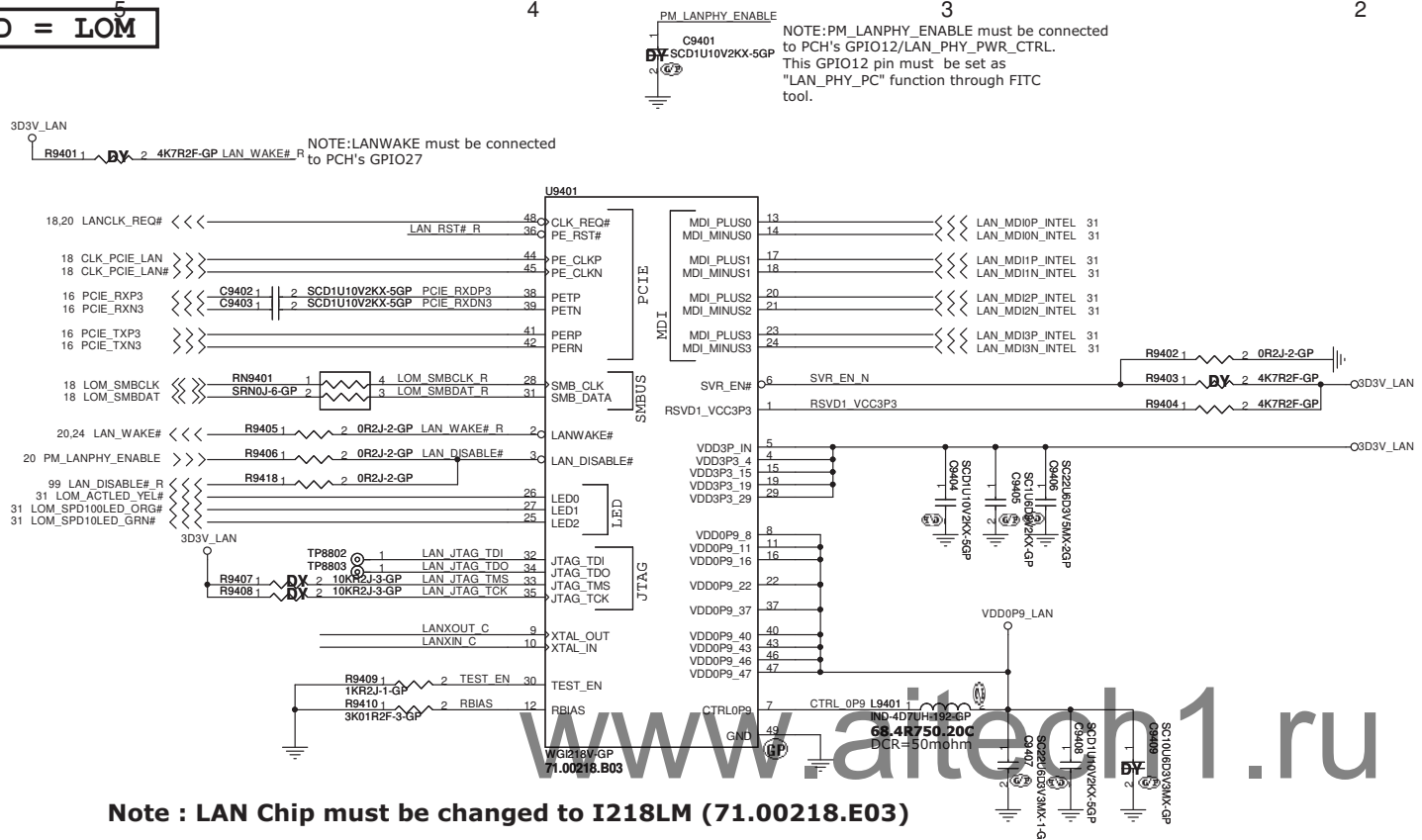
**Round Rock 13.3" UMA**

Rev  
**X00**

Date: Friday, June 28, 2013

Sheet 93 of 107

SSID = LOM

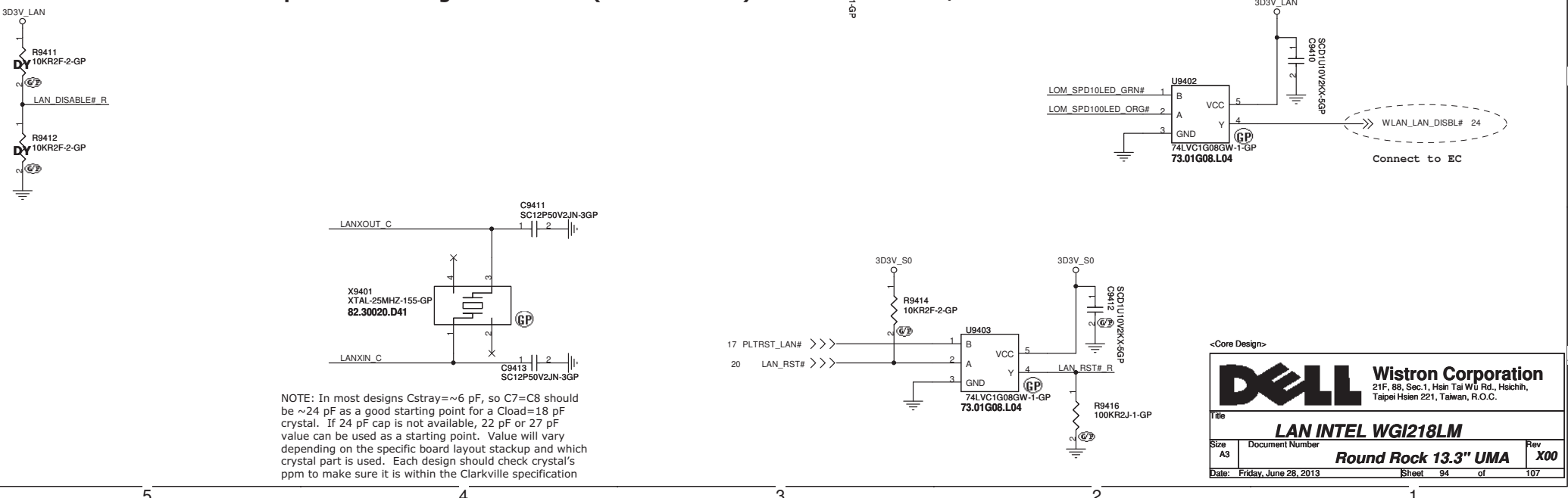


0D9V Power Options  
SVR\_EN\_N: Pull High External  
Pull Low Internal

Internal SVR	Shared with external 1.05V SVR
L9401: STUFF	L9401: NO STUFF
R9413: NO STUFF	R9413: STUFF
R9402: STUFF	R9402: NO STUFF
R9403: NO STUFF	R9403: STUFF

\*NOTE: Clarkville has 0.9V internal SVR. However it is also possible to disable this 0.9V iSVR and Clarkville can support the external 1.05V supply. When sharing, make sure the 1.05V\_LAN is controlled by the SLP\_LAN signal.

Note : LAN Chip must be changed to I218LM (71.00218.E03)



NOTE: In most designs Cstray= $\sim 6$  pF, so C7=C8 should be  $\sim 24$  pF as a good starting point for a Cload= $\sim 18$  pF crystal. If 24 pF cap is not available, 22 pF or 27 pF value can be used as a starting point. Value will vary depending on the specific board layout stackup and which crystal part is used. Each design should check crystal's ppm to make sure it is within the Clarkville specification

<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File **LAN INTEL WGI218LM**

Size A3	Document Number	Rev X00
Date: Friday, June 28, 2013	Sheet 94 of 107	

(Blanking)

www.aitech1.ru

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**LAN SW**

Size  
A4

Document Number

**Round Rock 13.3" UMA**

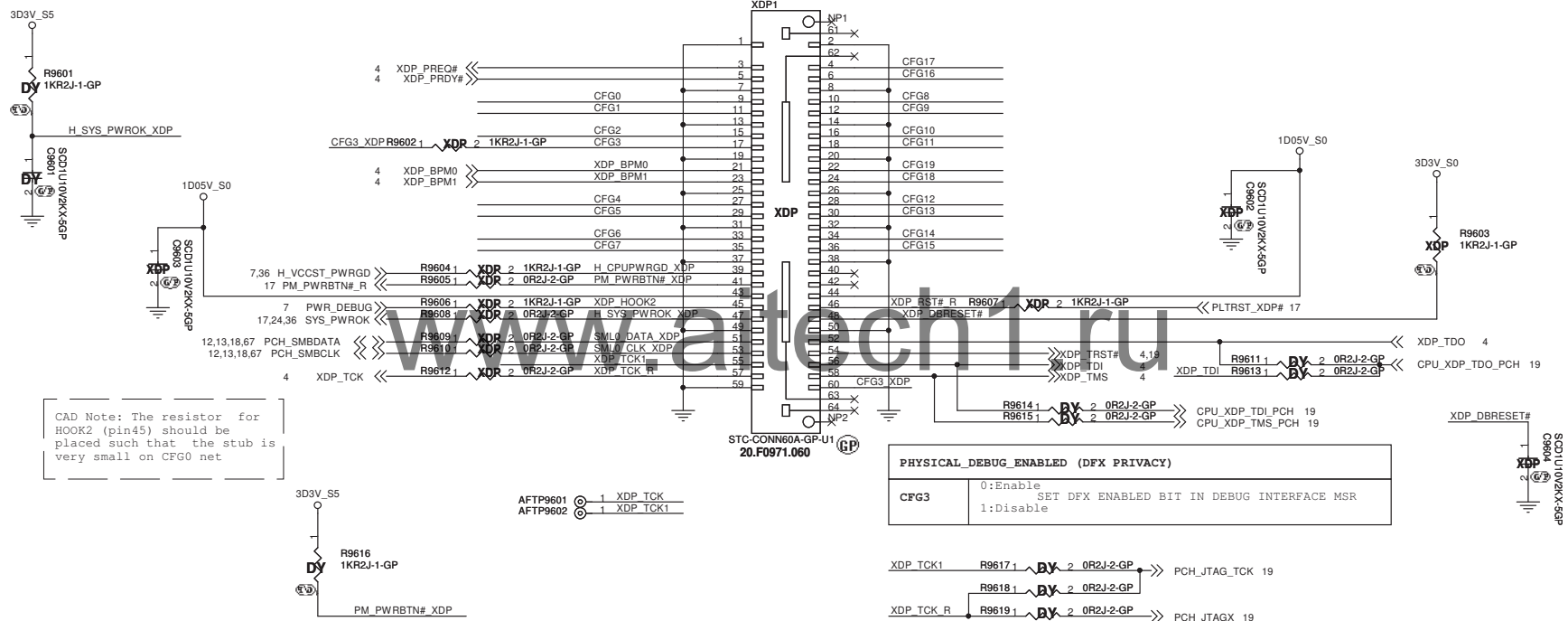
Rev  
**X00**

Date: Friday, June 28, 2013

Sheet 95 of 107

SSID = CPU\_XDP

## CPU\_XDP



<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>CPU_XDP</b>
Size	Document Number	Rev	
A3		X00	
Date: Friday, June 28, 2013			Sheet 96 of 107

(Blanking)

www.altech1.ru

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**USB2.0 HUB**

Size  
A4

Document Number

**Round Rock 13.3" UMA**

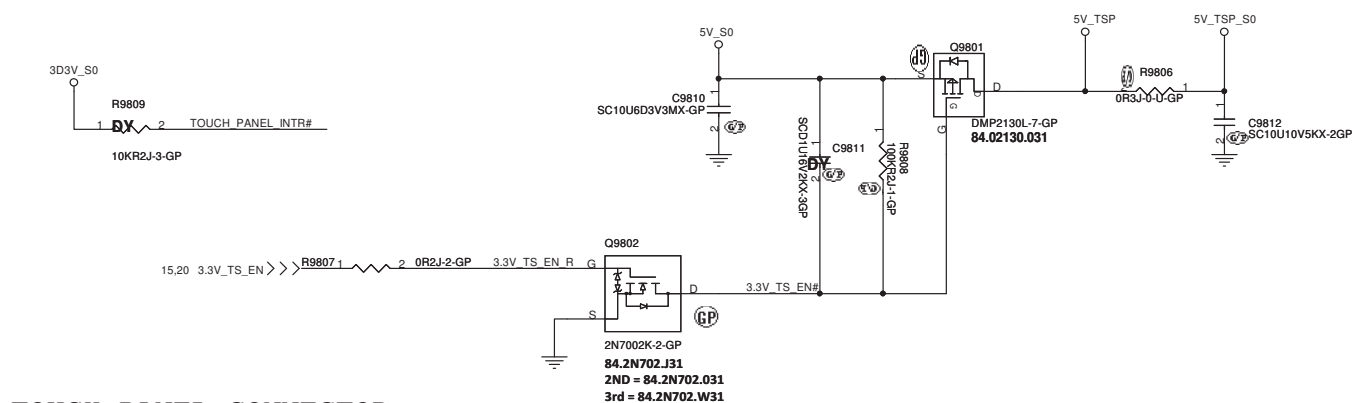
Rev  
**X00**

Date: Friday, June 28, 2013

Sheet 97 of 107

```
SSID = User.Interface
```

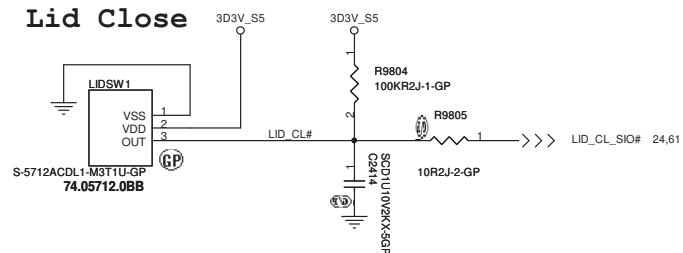
## TOUCH PANEL POWER



## TOUCH PANEL CONNECTOR



Lid Close



### <Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

### Function Button

Size	Document Number
------	-----------------

### Round Rock 13.3" UMA

Rev

Date: Friday, June 28, 2013

Sheet 98 of

---

107

